INSPECTUS

FIG. 1

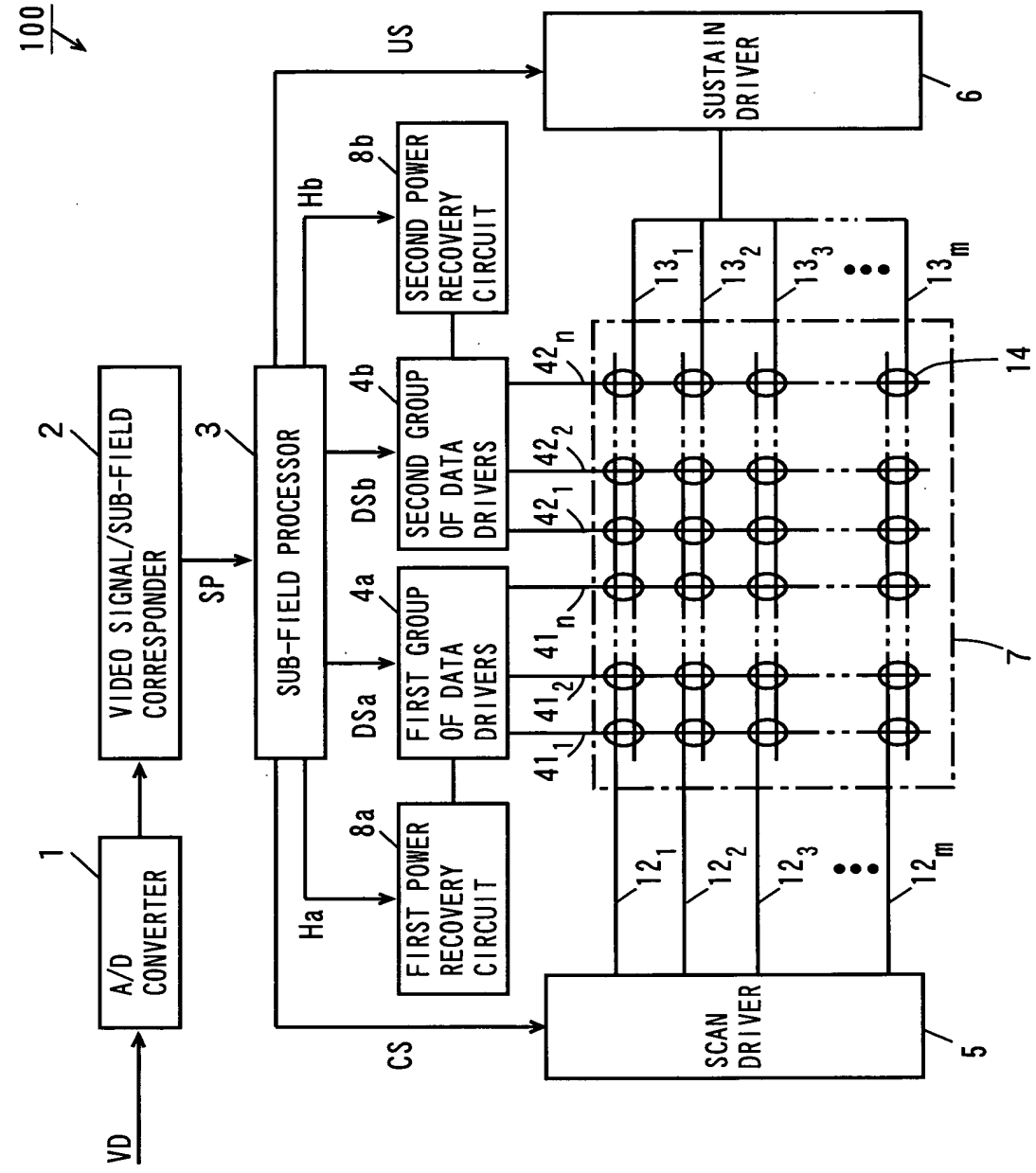


FIG. 2

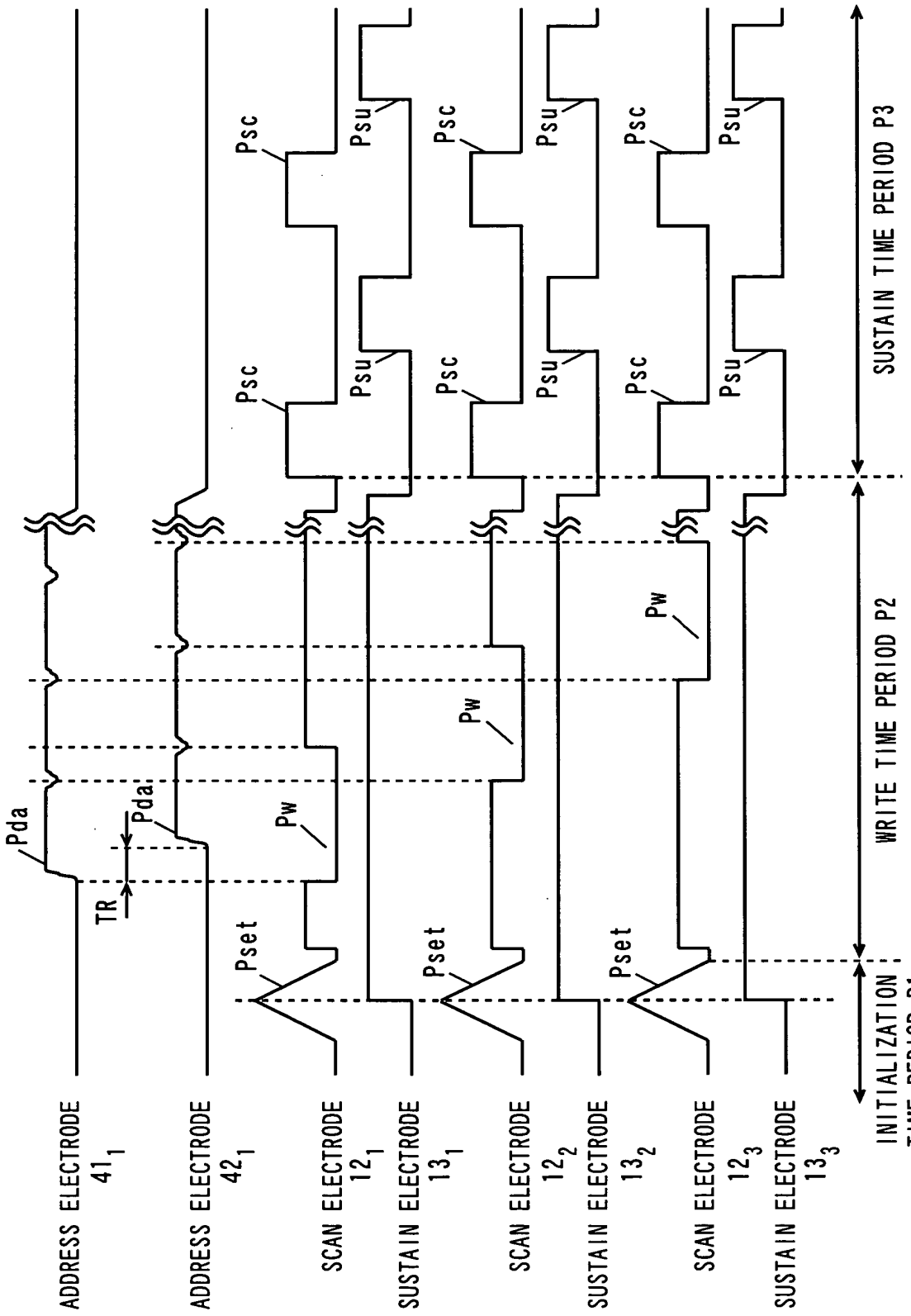

ADDRESS ELECTRODE 41_1
ADDRESS ELECTRODE 42_1
SCAN ELECTRODE 12_1
SUSTAIN ELECTRODE 13_1
SCAN ELECTRODE 12_2
SUSTAIN ELECTRODE 13_2
SCAN ELECTRODE 12_3
SUSTAIN ELECTRODE 13_3
Pda
Pda
TR
Pset
Pw
Psc
Psu
INITIALIZATION TIME PERIOD P1
WRITE TIME PERIOD P2
SUSTAIN TIME PERIOD P3

FIG. 3

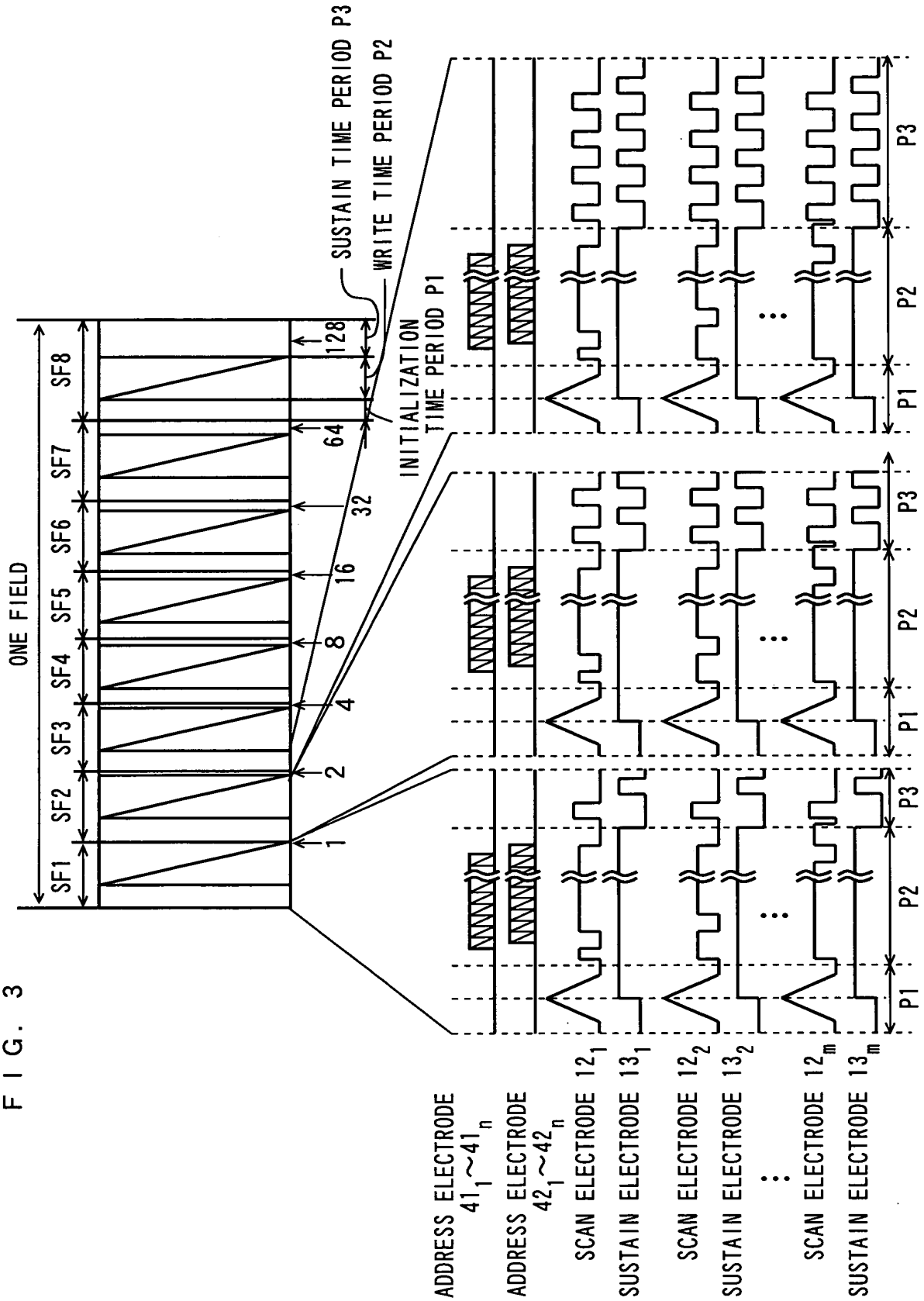

ONE FIELD
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
1
2
4
8
16
32
64
128
SUSTAIN TIME PERIOD P3
WRITE TIME PERIOD P2
INITIALIZATION TIME PERIOD P1
ADDRESS ELECTRODE 41_1~41_n
ADDRESS ELECTRODE 42_1~42_n
SCAN ELECTRODE 12_1
SUSTAIN ELECTRODE 13_1
SCAN ELECTRODE 12_2
SUSTAIN ELECTRODE 13_2
SCAN ELECTRODE 12_m
SUSTAIN ELECTRODE 13_m
P1
P2
P3

FIG. 4

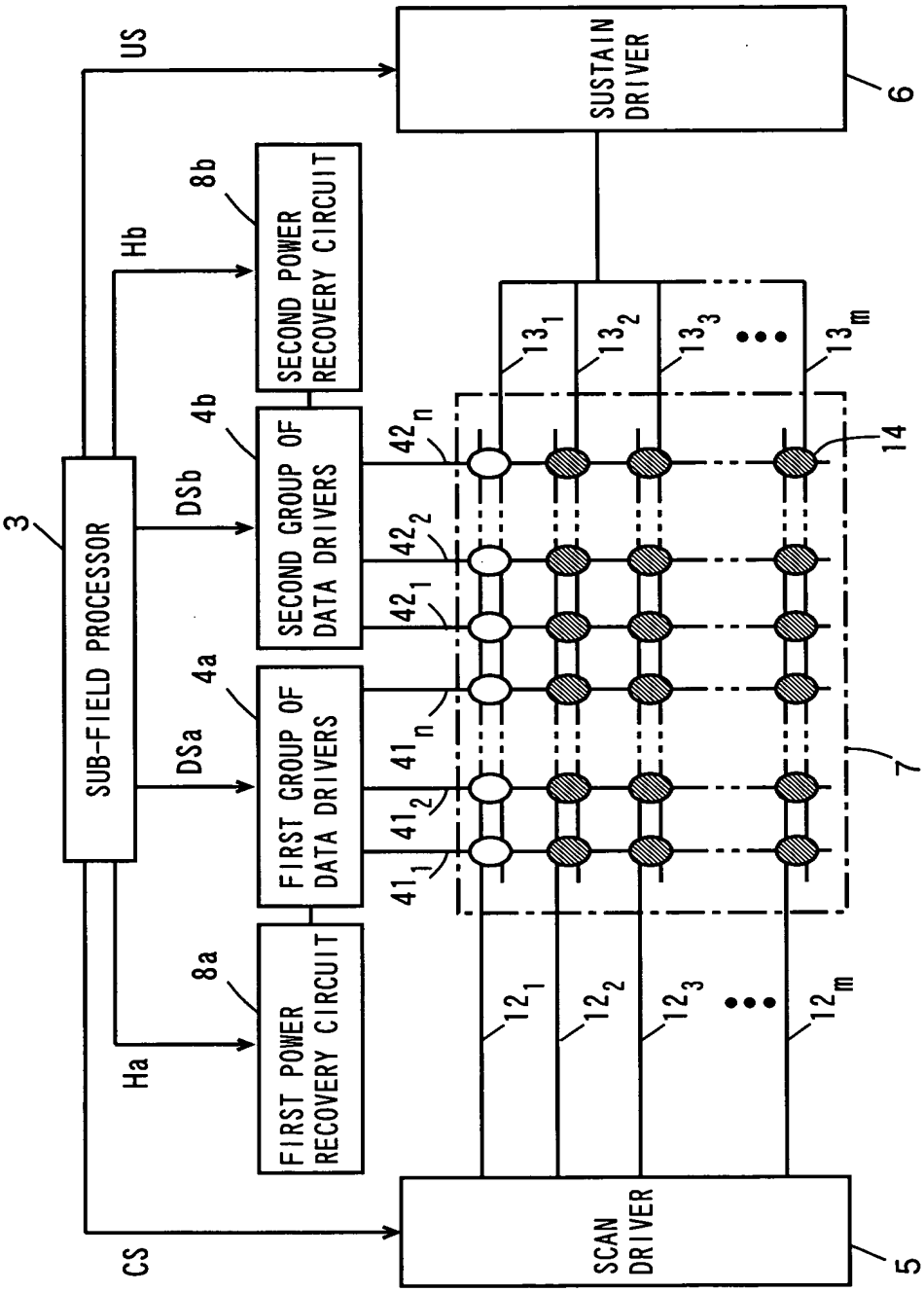

SUSTAIN DRIVER
6
US
Hb
8b
SECOND POWER RECOVERY CIRCUIT
4b
SECOND GROUP OF DATA DRIVERS
DSb
3
SUB-FIELD PROCESSOR
DSa
4a
FIRST GROUP OF DATA DRIVERS
Ha
8a
FIRST POWER RECOVERY CIRCUIT
CS
SCAN DRIVER
5
13_1
13_2
13_3
13_m
14
7
42_n
42_2
42_1
41_n
41_2
41_1
12_1
12_2
12_3
12_m

FIG. 5

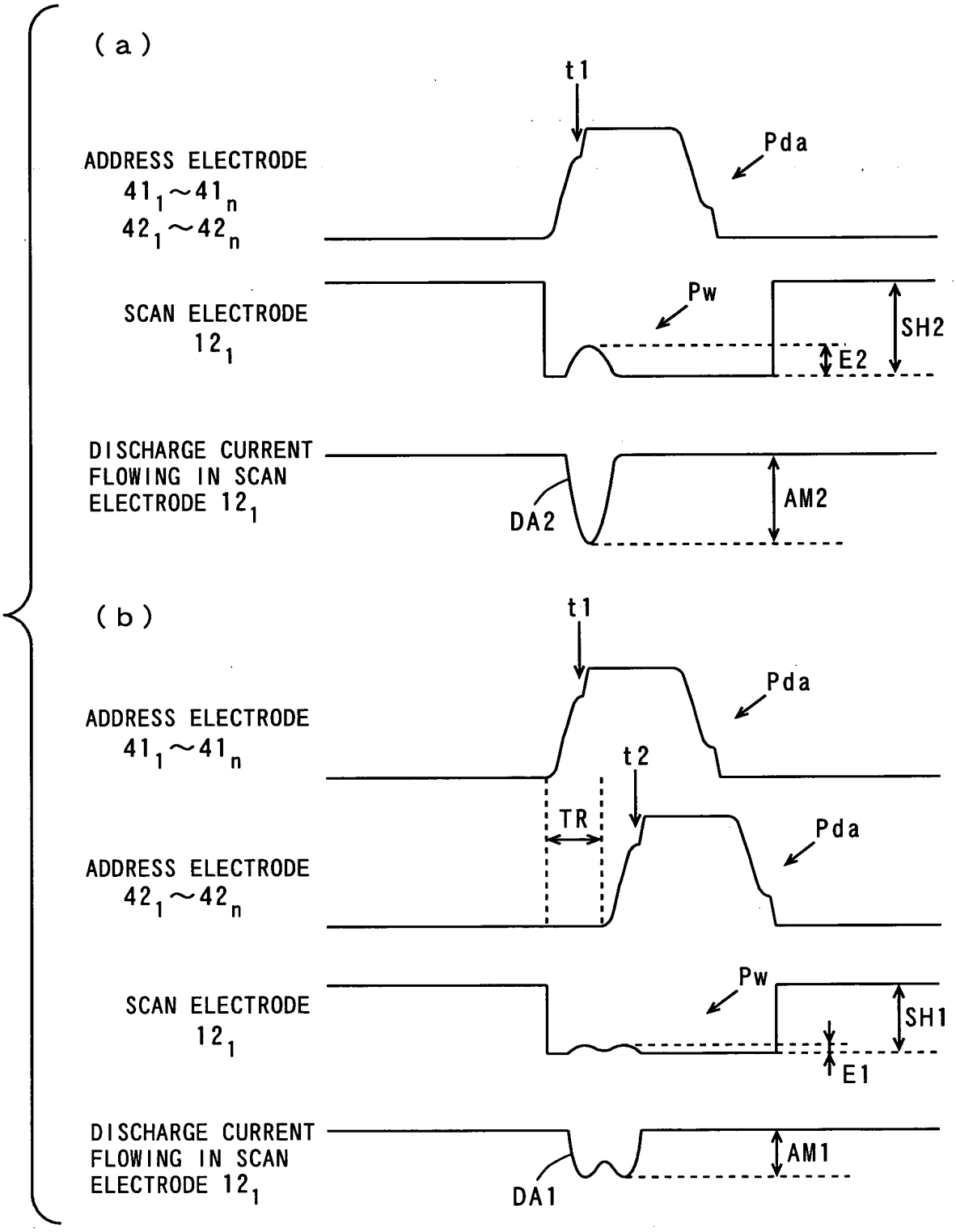

(a)
t1
Pda
ADDRESS ELECTRODE
41₁~41ₙ
42₁~42ₙ
SCAN ELECTRODE
12₁
Pw
SH2
E2
DISCHARGE CURRENT
FLOWING IN SCAN
ELECTRODE 12₁
DA2
AM2
(b)
t1
Pda
ADDRESS ELECTRODE
41₁~41ₙ
t2
TR
Pda
ADDRESS ELECTRODE
42₁~42ₙ
Pw
SCAN ELECTRODE
12₁
SH1
E1
DISCHARGE CURRENT
FLOWING IN SCAN
ELECTRODE 12₁
DA1
AM1

FIG. 6

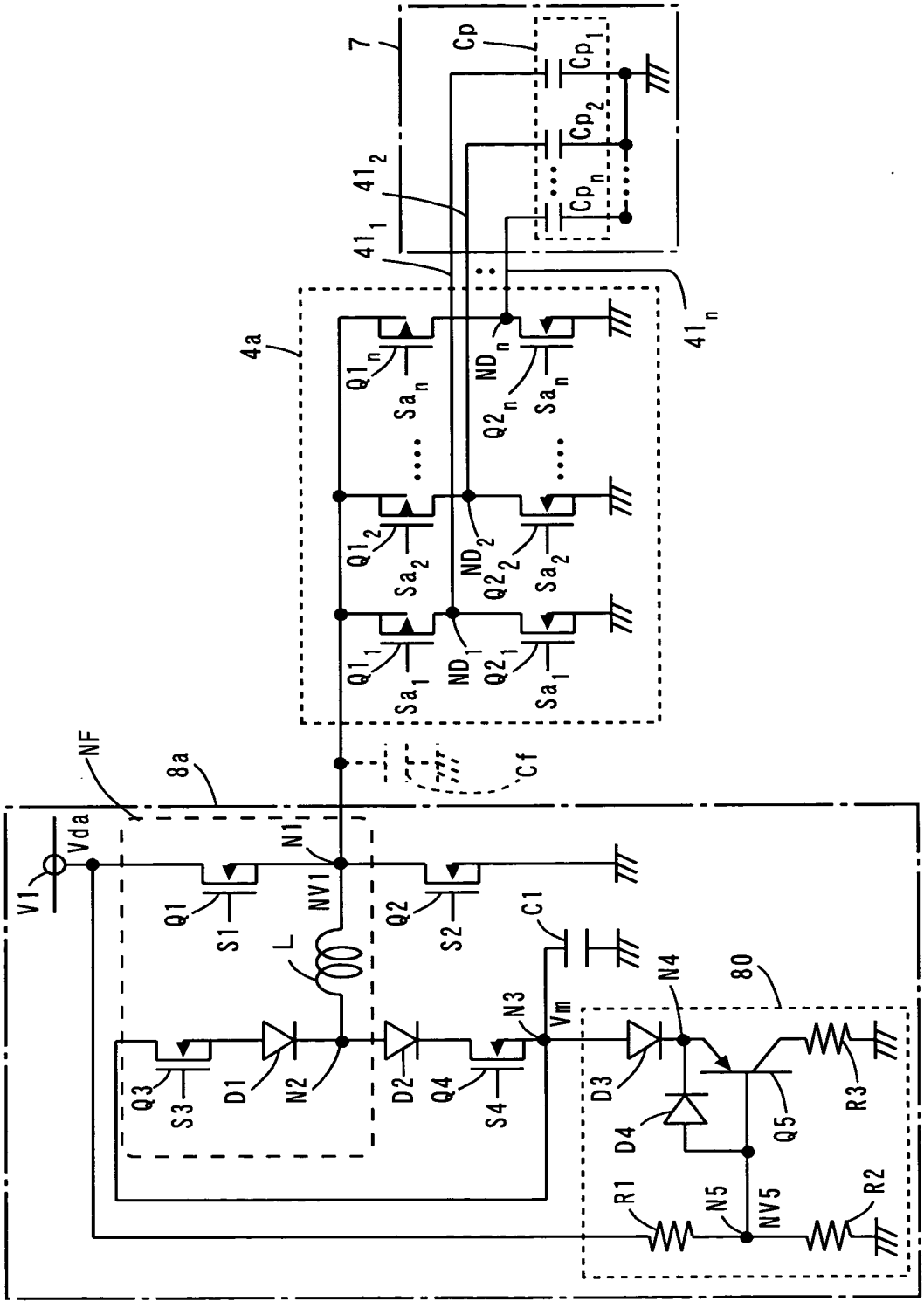
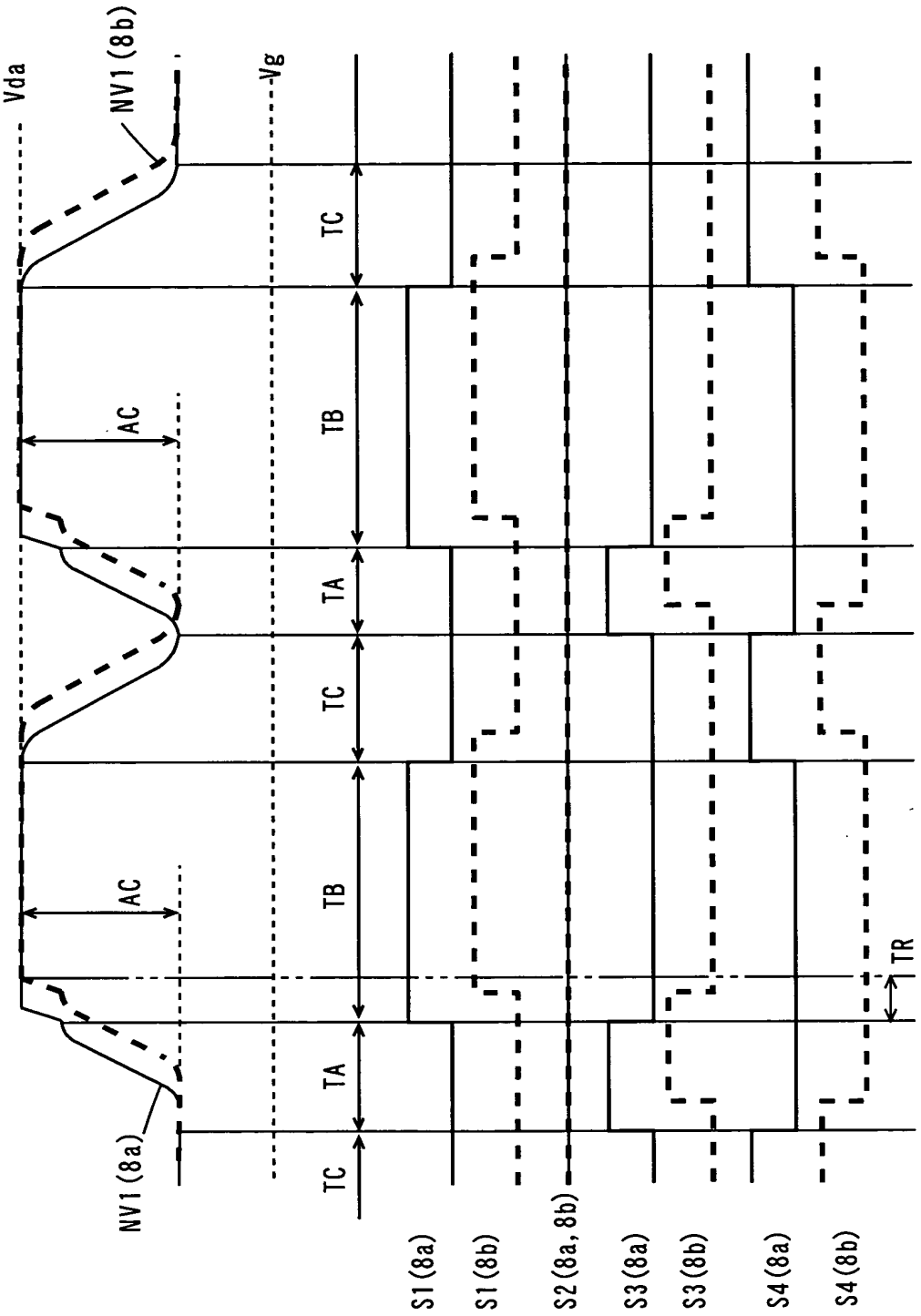

7
Cp
Cp1
Cp2
Cpn
412
411
41n
4a
Q1n
Can
NDn
Q2n
Q12
Ca2
ND2
Q22
Q11
Ca1
ND1
Q21
Cf
NF
8a
Vda
V1
N11
Q1
S1
NV1
Q2
S2
C1
L
N4
80
N3
Vm
Q3
S3
D1
N2
D2
Q4
S4
D3
D4
Q5
R3
R1
N5
NV5
R2

FIG. 7


Vda
NV1(8b)
Vg
TC
TB
AC
TA
TC
TB
AC
TA
TC
NV1(8a)
TR
S1(8a)
S1(8b)
S2(8a,8b)
S3(8a)
S3(8b)
S4(8a)
S4(8b)

F I G. 8

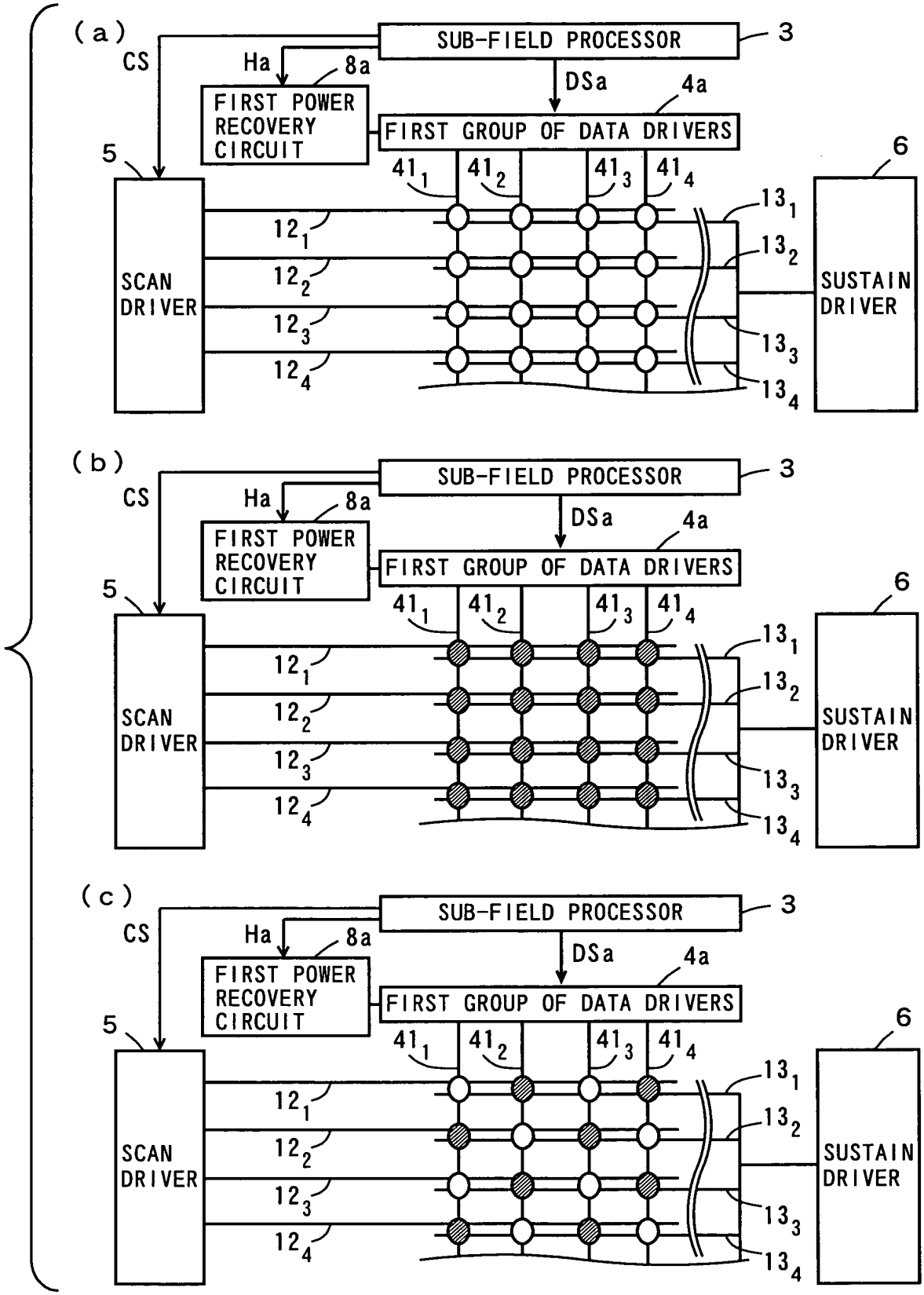

(a)
CS
Ha
8a
SUB-FIELD PROCESSOR
3
DSa
4a
FIRST POWER RECOVERY CIRCUIT
FIRST GROUP OF DATA DRIVERS
5
6
41_1
41_2
41_3
41_4
13_1
13_2
13_3
13_4
12_1
12_2
12_3
12_4
SCAN DRIVER
SUSTAIN DRIVER
(b)
CS
Ha
8a
SUB-FIELD PROCESSOR
3
DSa
4a
FIRST POWER RECOVERY CIRCUIT
FIRST GROUP OF DATA DRIVERS
5
6
41_1
41_2
41_3
41_4
13_1
13_2
13_3
13_4
12_1
12_2
12_3
12_4
SCAN DRIVER
SUSTAIN DRIVER
(c)
CS
Ha
8a
SUB-FIELD PROCESSOR
3
DSa
4a
FIRST POWER RECOVERY CIRCUIT
FIRST GROUP OF DATA DRIVERS
5
6
41_1
41_2
41_3
41_4
13_1
13_2
13_3
13_4
12_1
12_2
12_3
12_4
SCAN DRIVER
SUSTAIN DRIVER

FIG. 9

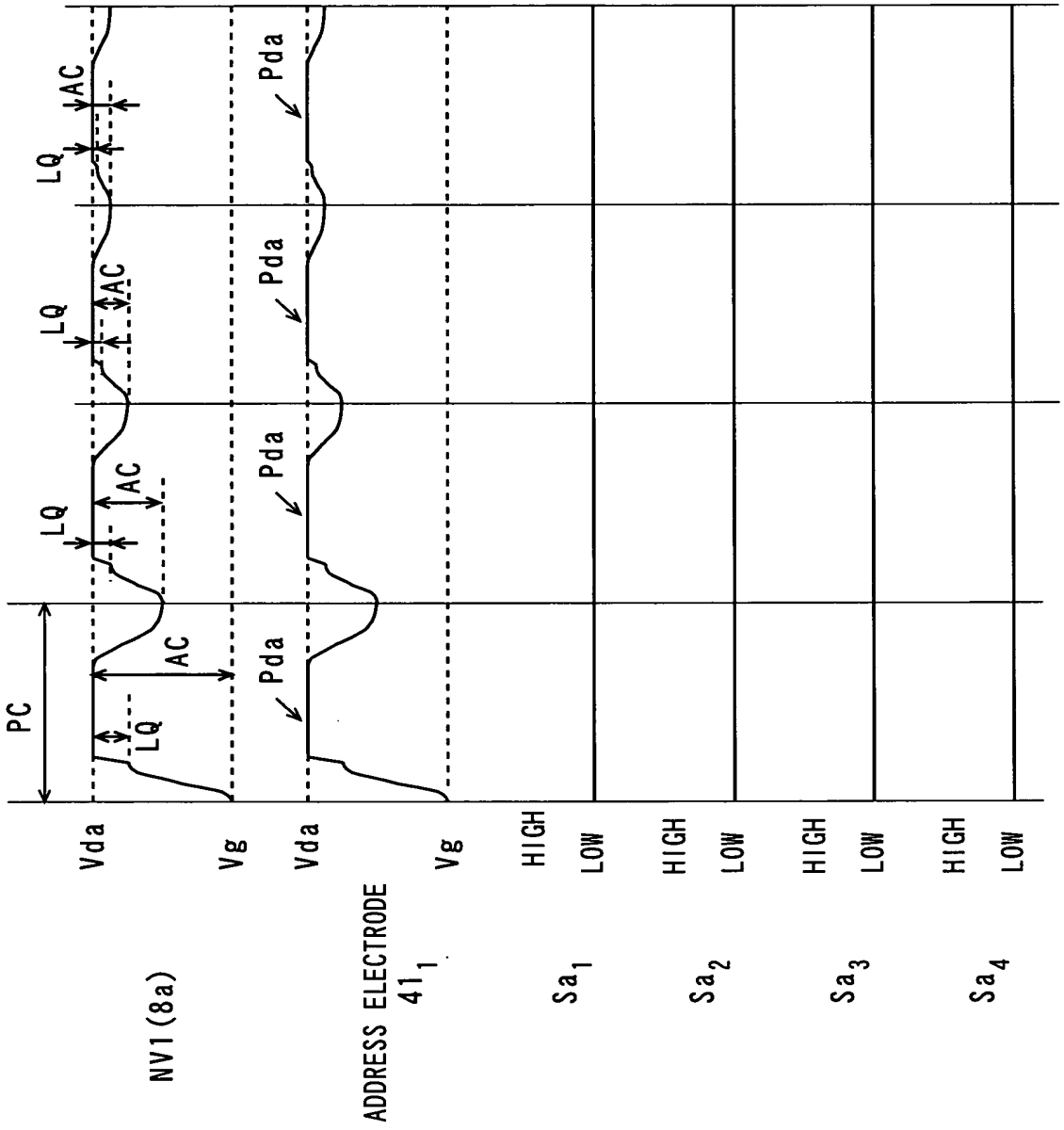

PC
LQ
AC
Pda
Vda
Vg
HIGH
LOW
NV1(8a)
ADDRESS ELECTRODE 41$_1$
Sa$_1$
Sa$_2$
Sa$_3$
Sa$_4$

FIG. 10

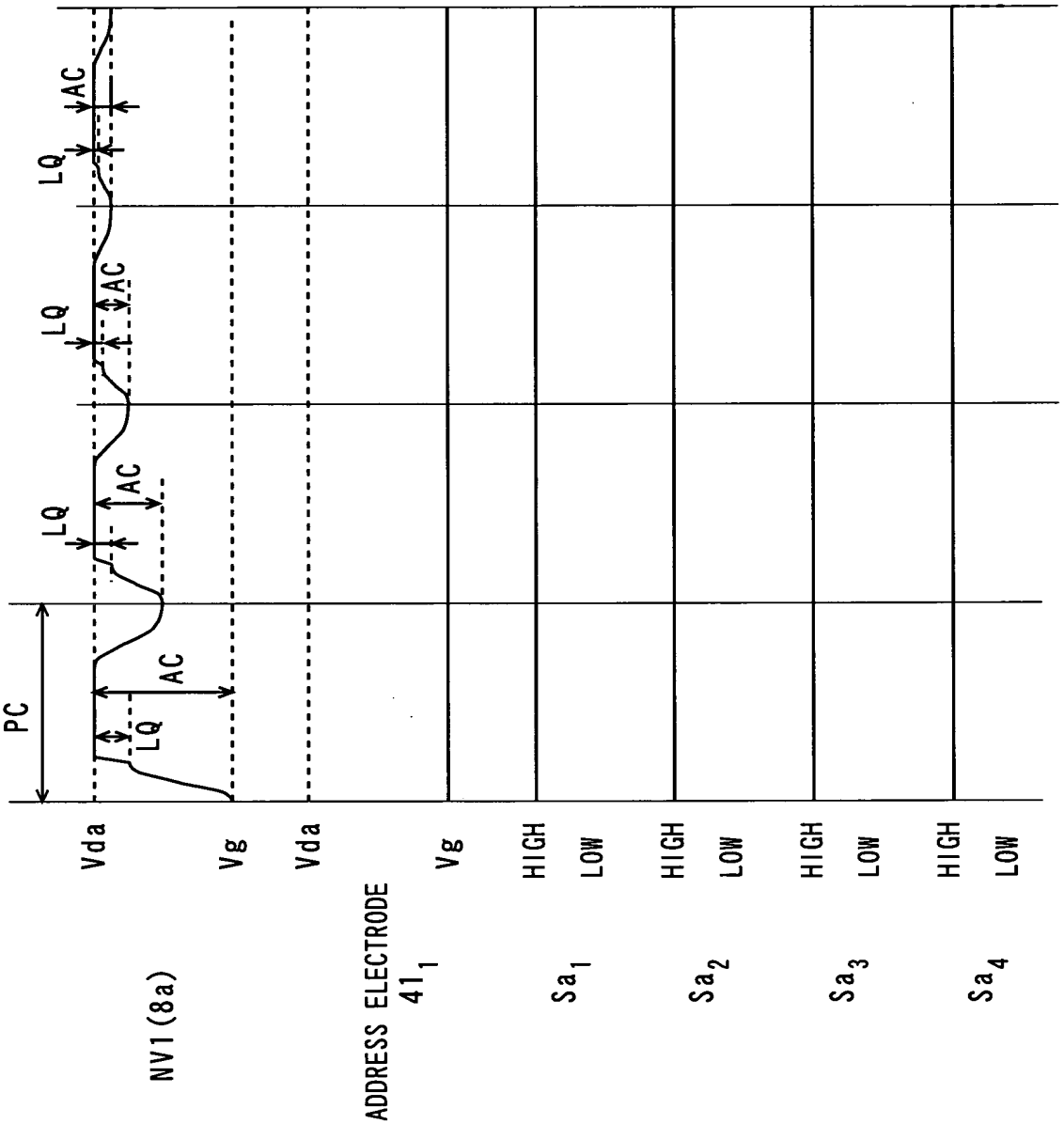

PC
LQ
AC
Vda
Vg
NV1(8a)
ADDRESS ELECTRODE
41 1
HIGH
LOW
Sa 1
Sa 2
Sa 3
Sa 4

FIG. 11

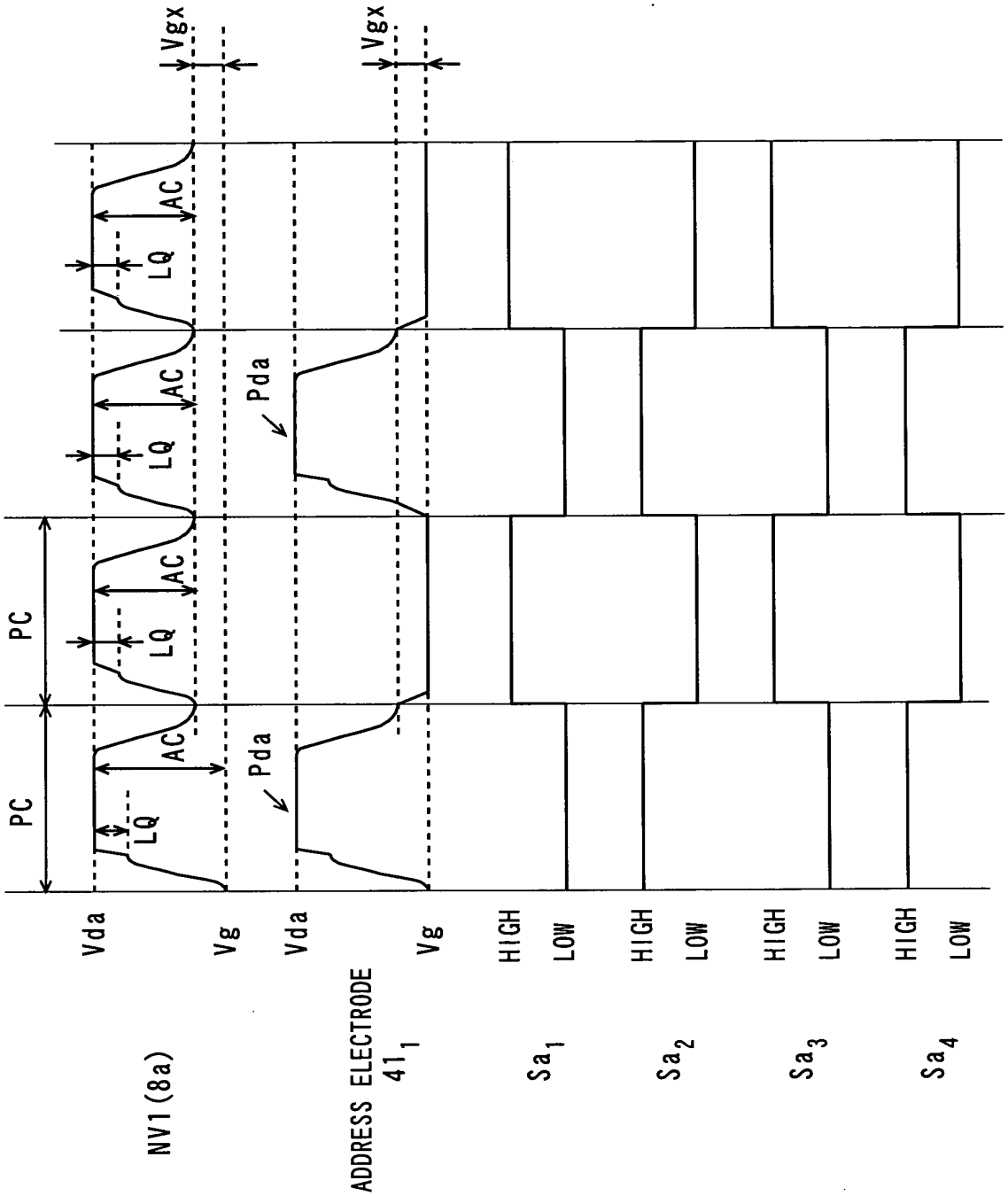

Vgx
Vgx
PC
PC
LQ
AC
Pda
Vda
Vg
Vda
Vg
HIGH
LOW
NV1(8a)
ADDRESS ELECTRODE 41$_1$
Sa$_1$
Sa$_2$
Sa$_3$
Sa$_4$

FIG. 12

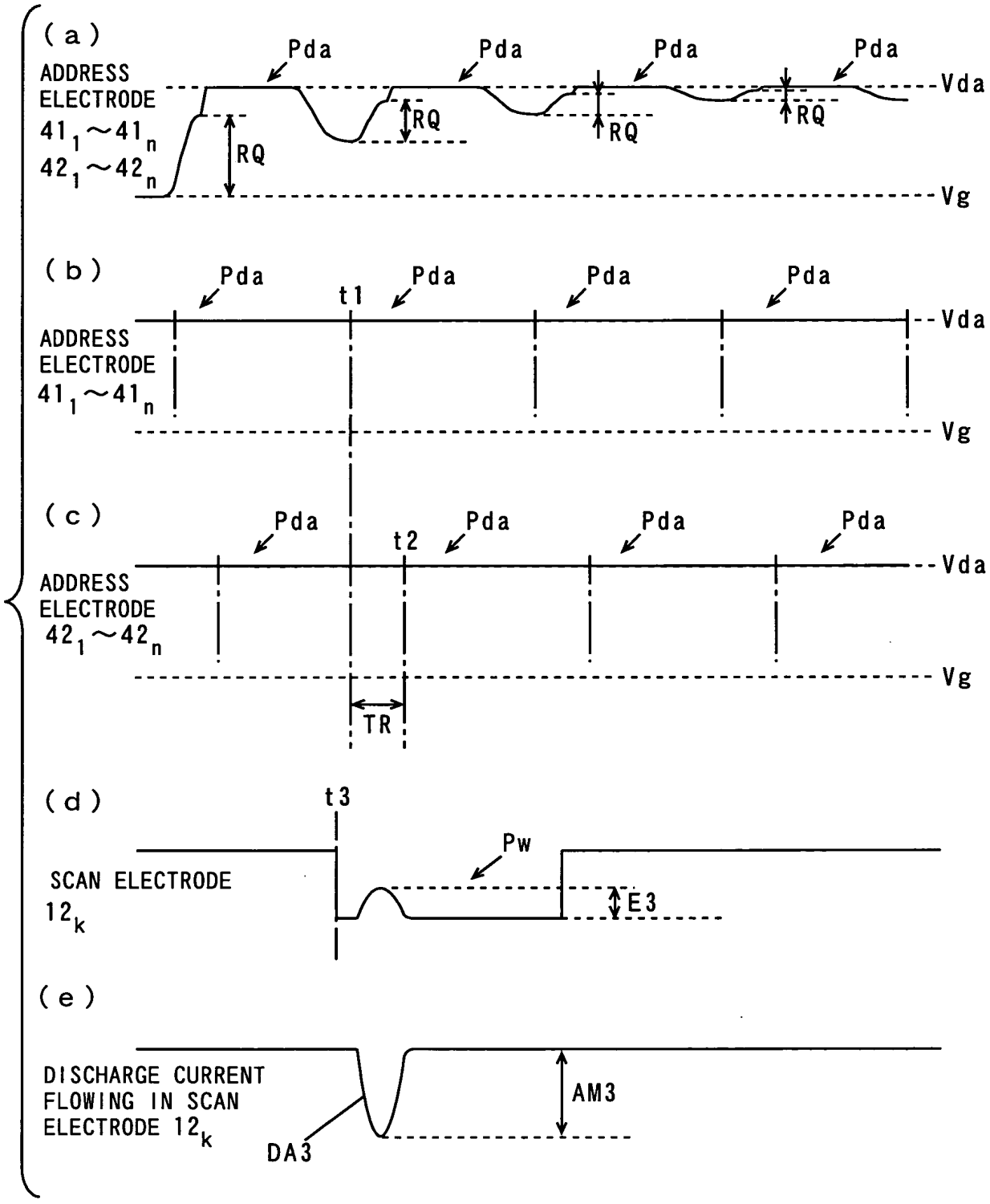

(a)
ADDRESS ELECTRODE 41₁～41ₙ 42₁～42ₙ
Pda
RQ
Vda
Vg
(b)
t1
ADDRESS ELECTRODE 41₁～41ₙ
(c)
t2
ADDRESS ELECTRODE 42₁～42ₙ
TR
(d)
t3
Pw
SCAN ELECTRODE 12ₖ
E3
(e)
DISCHARGE CURRENT FLOWING IN SCAN ELECTRODE 12ₖ
AM3
DA3

FIG. 13

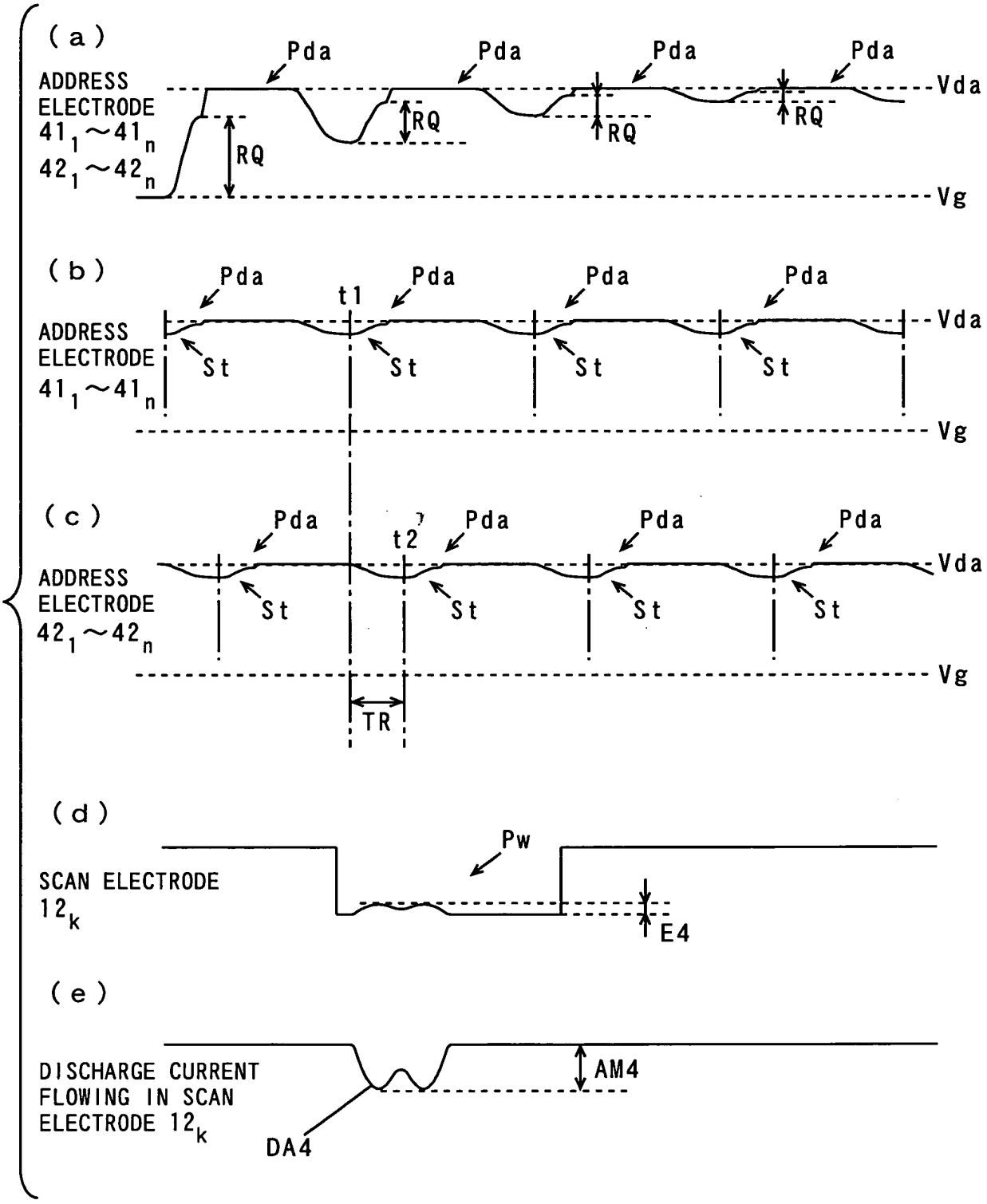

(a)
ADDRESS ELECTRODE 41₁~41ₙ 42₁~42ₙ
Pda
RQ
Vda
Vg
(b)
ADDRESS ELECTRODE 41₁~41ₙ
t1
St
(c)
ADDRESS ELECTRODE 42₁~42ₙ
t2
TR
(d)
SCAN ELECTRODE 12ₖ
Pw
E4
(e)
DISCHARGE CURRENT FLOWING IN SCAN ELECTRODE 12ₖ
AM4
DA4

FIG. 14

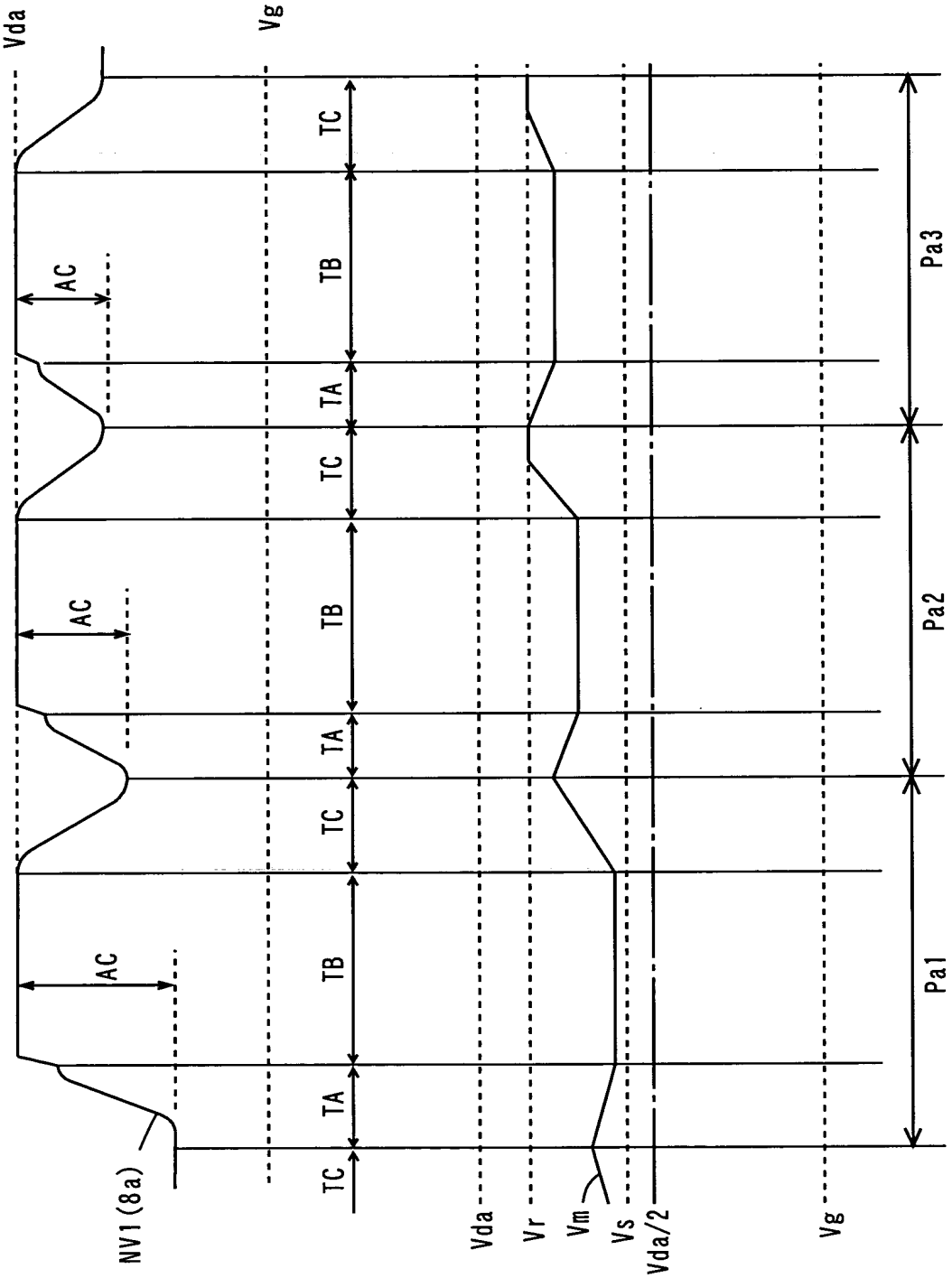


FIG. 15

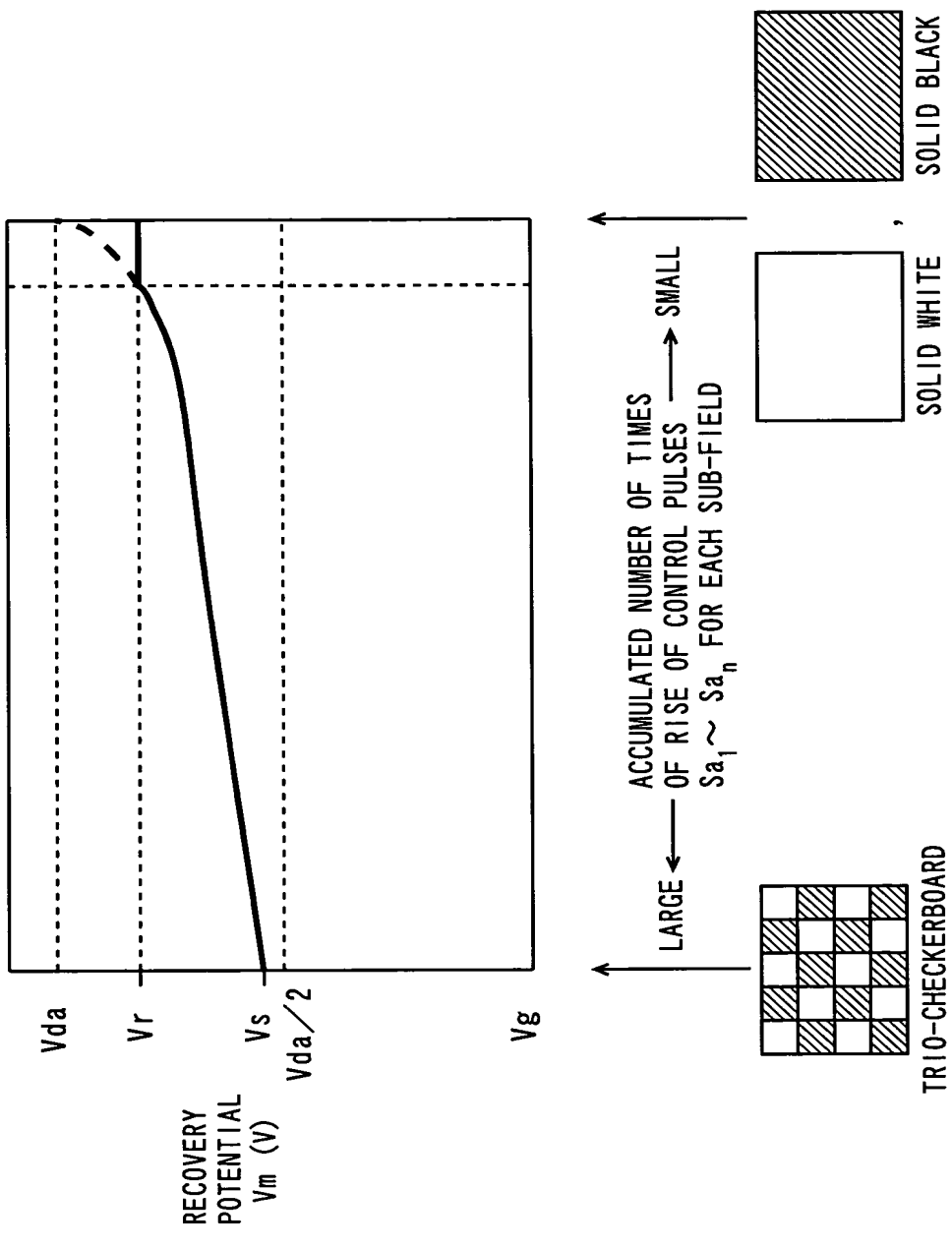
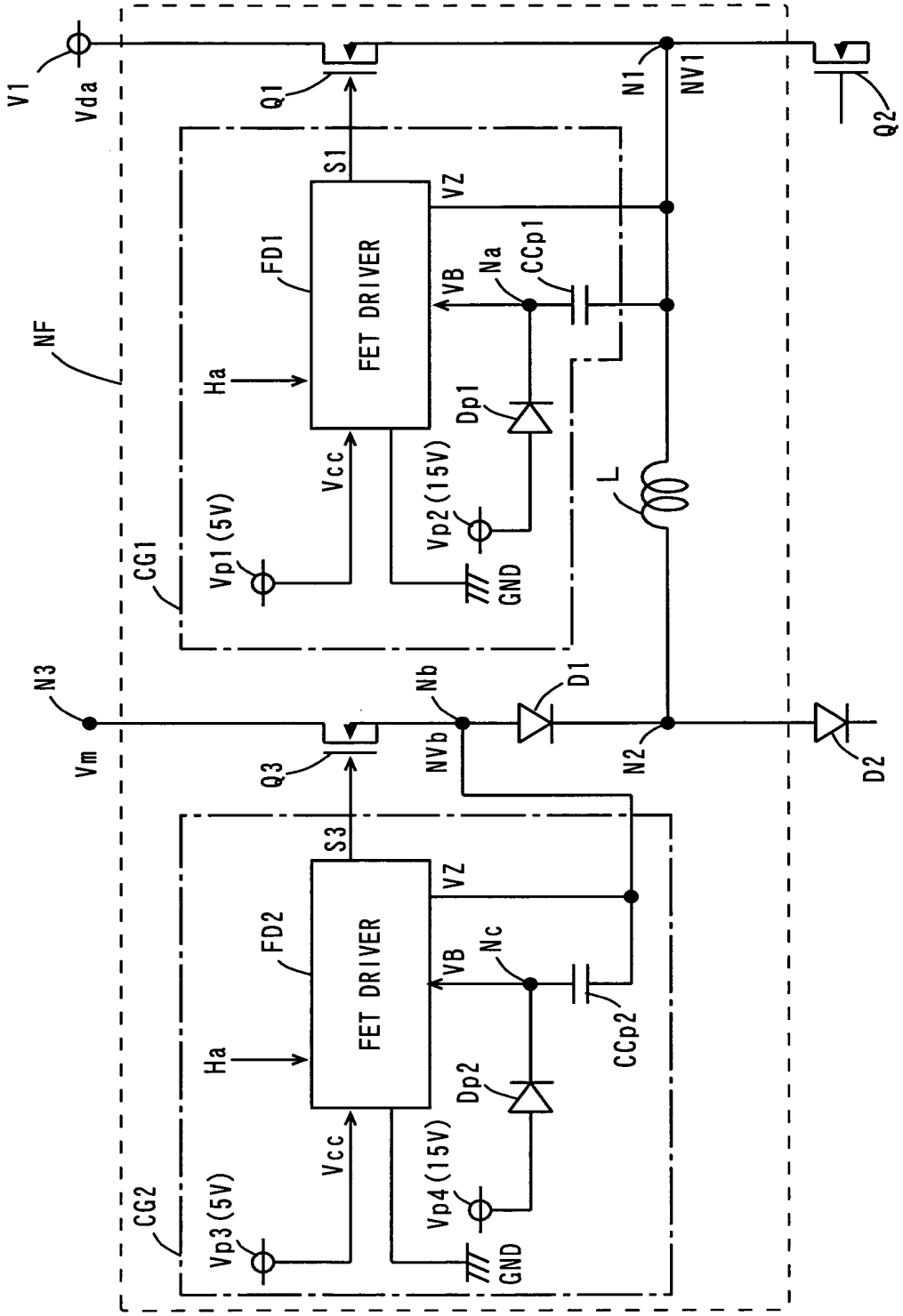

Vda
Vr
Vs
Vda/2
Vg
RECOVERY POTENTIAL Vm (V)
LARGE ← ACCUMULATED NUMBER OF TIMES OF RISE OF CONTROL PULSES → SMALL
Sa1 ~ San FOR EACH SUB-FIELD
TRIO-CHECKERBOARD
SOLID WHITE
SOLID BLACK

FIG. 16


V1
Vda
Q1
N1
NV1
Q2
S1
VZ
FD1
FET DRIVER
VB
Na
CCp1
NF
Ha
Dp1
Vcc
Vp2(15V)
L
Vp1(5V)
GND
CG1
N3
Nb
D1
Vm
Q3
NVb
N2
D2
S3
VZ
FD2
FET DRIVER
VB
Nc
CCp2
Ha
Dp2
Vcc
Vp4(15V)
Vp3(5V)
GND
CG2

F I G. 1 7

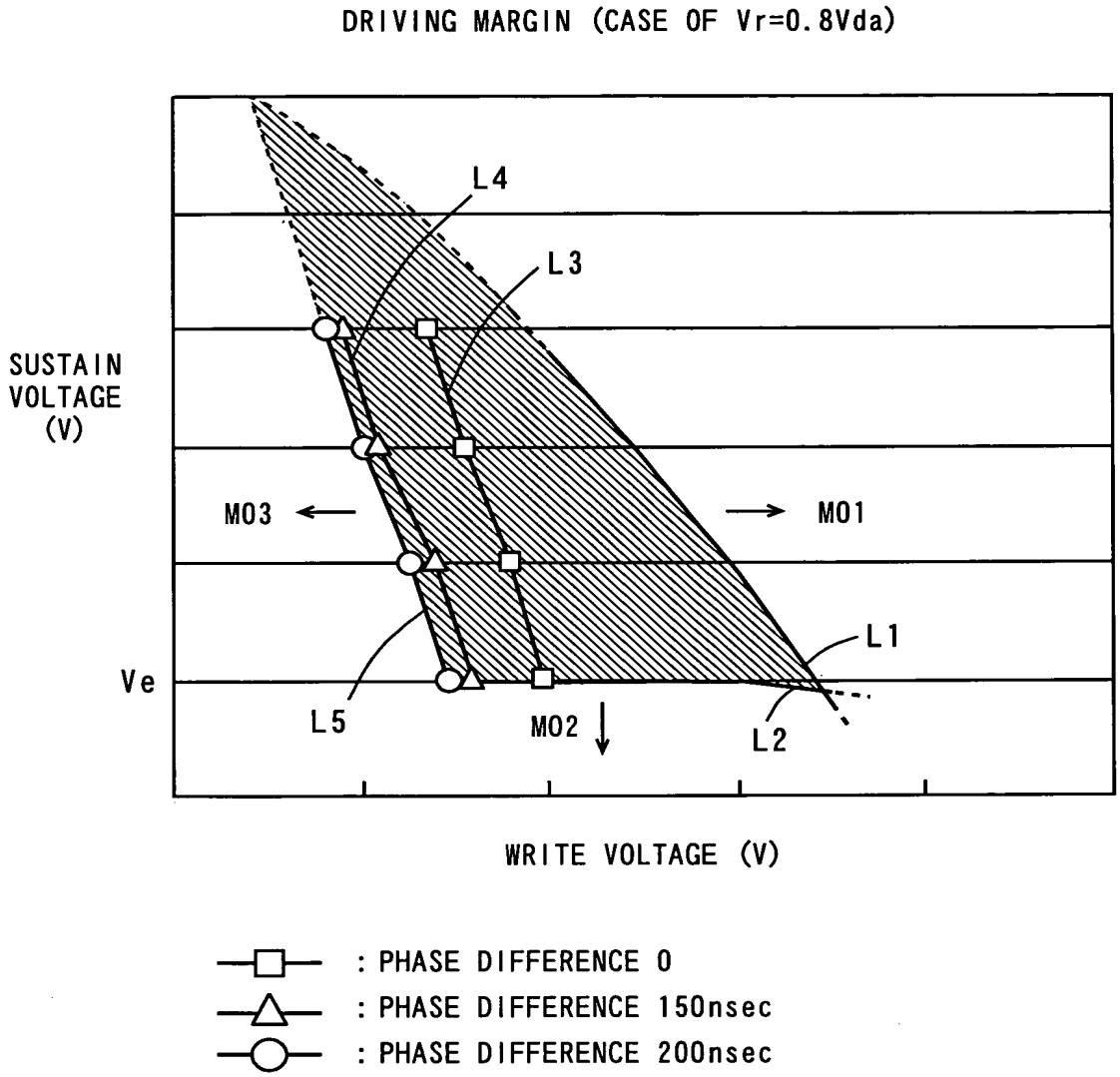

DRIVING MARGIN (CASE OF Vr=0.8Vda)
SUSTAIN VOLTAGE (V)
L4
L3
M03
M01
L1
Ve
L5
M02
L2
WRITE VOLTAGE (V)
: PHASE DIFFERENCE 0
: PHASE DIFFERENCE 150nsec
: PHASE DIFFERENCE 200nsec

FIG. 18

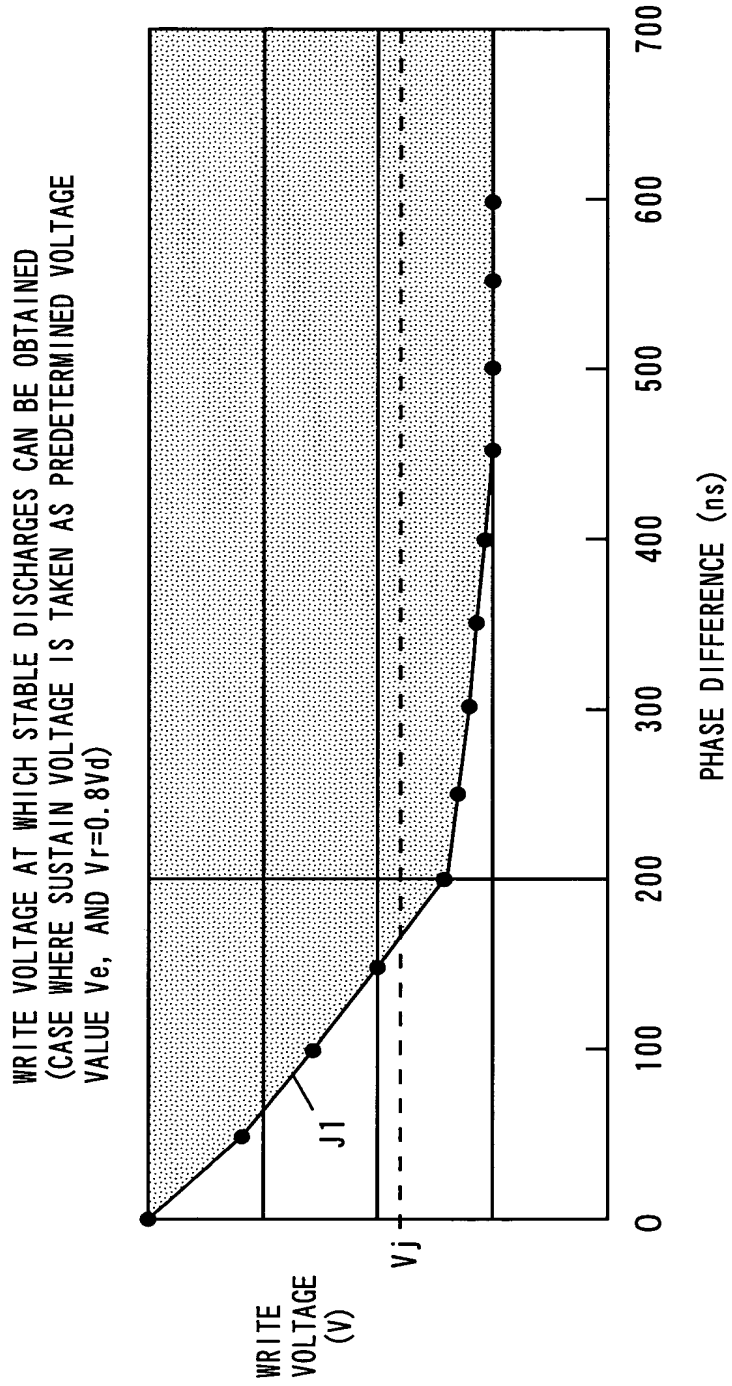

WRITE VOLTAGE AT WHICH STABLE DISCHARGES CAN BE OBTAINED
(CASE WHERE SUSTAIN VOLTAGE IS TAKEN AS PREDETERMINED VOLTAGE VALUE Ve, AND Vr=0.8Vd)
WRITE VOLTAGE (V)
Vj
J1
0
100
200
300
400
500
600
700
PHASE DIFFERENCE (ns)

FIG. 19

WRITE VOLTAGE AT WHICH STABLE DISCHARGES CAN BE OBTAINED
(CASE WHERE SUSTAIN VOLTAGE IS TAKEN AS PREDETERMINED VOLTAGE
VALUE Ve, AND PHASE DIFFERENCE IS TAKEN AS 200ns)

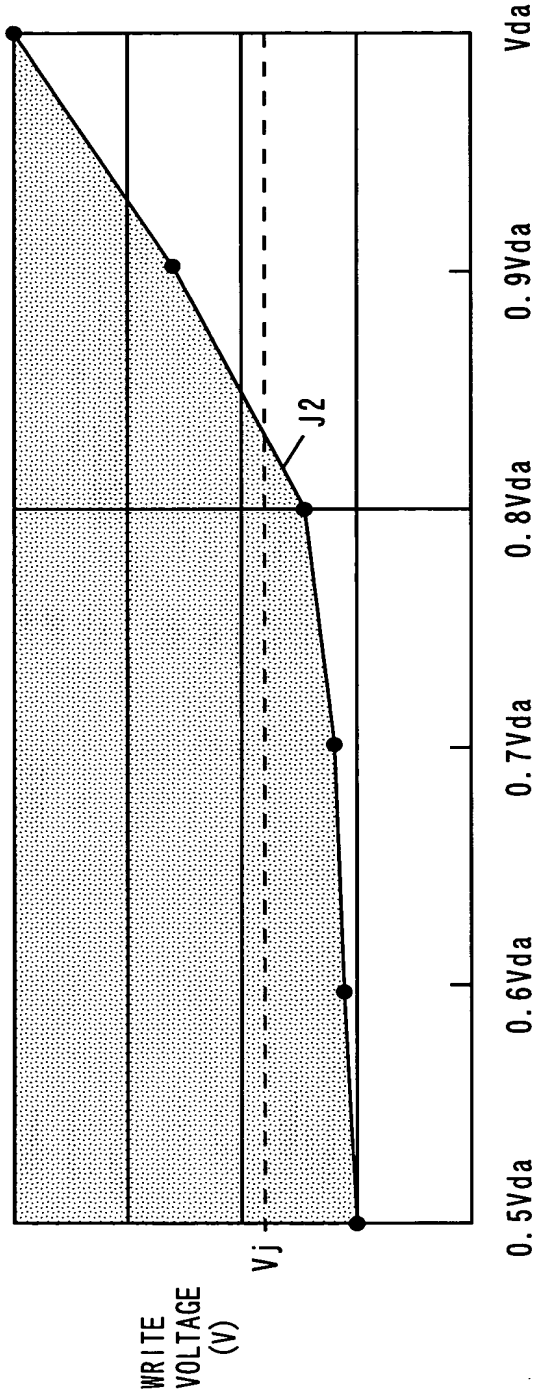


FIG. 20

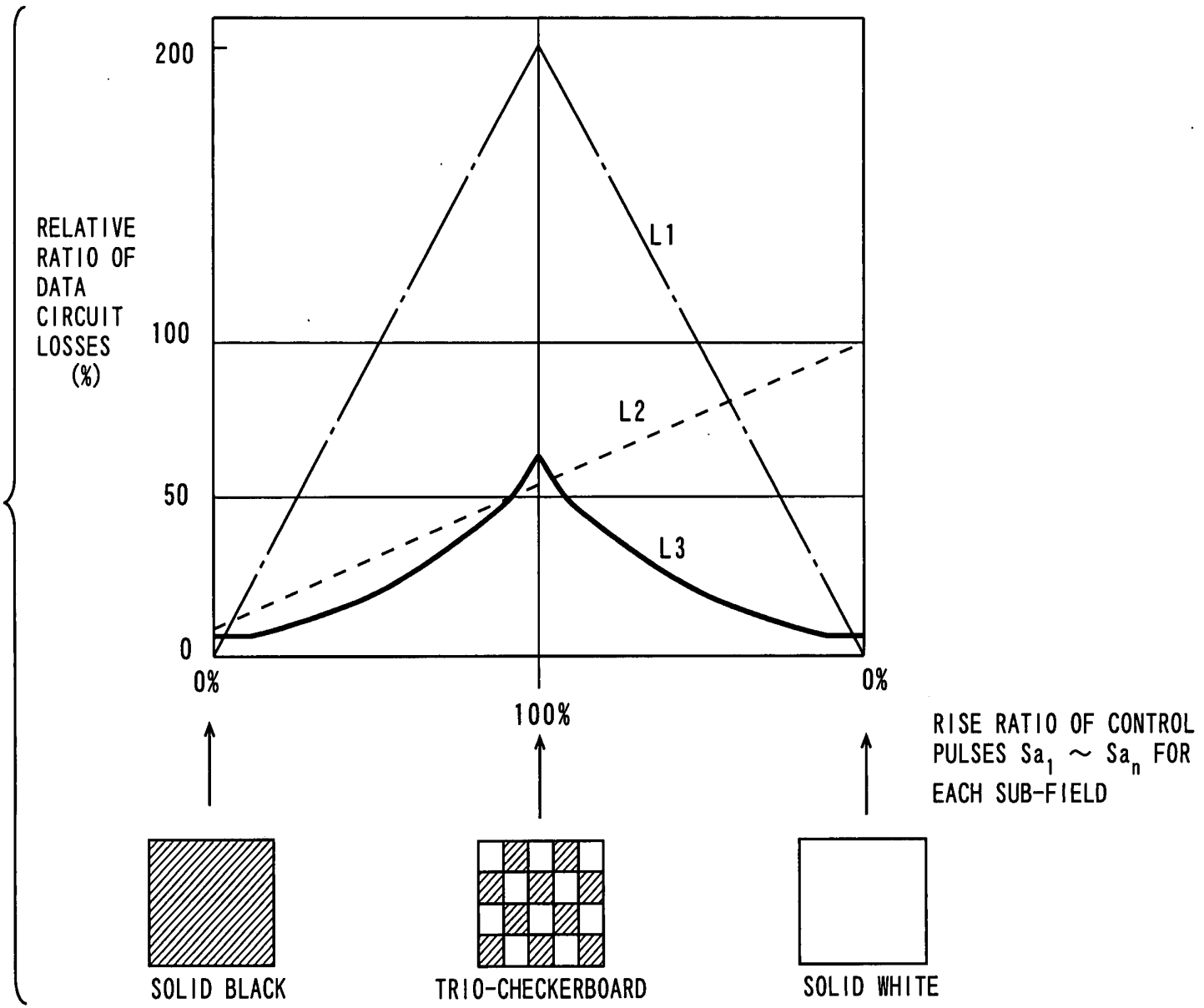

200
100
50
0
RELATIVE RATIO OF DATA CIRCUIT LOSSES (%)
L1
L2
L3
0%
100%
0%
RISE RATIO OF CONTROL PULSES $Sa_1 \sim Sa_n$ FOR EACH SUB-FIELD
SOLID BLACK
TRIO-CHECKERBOARD
SOLID WHITE

FIG. 21

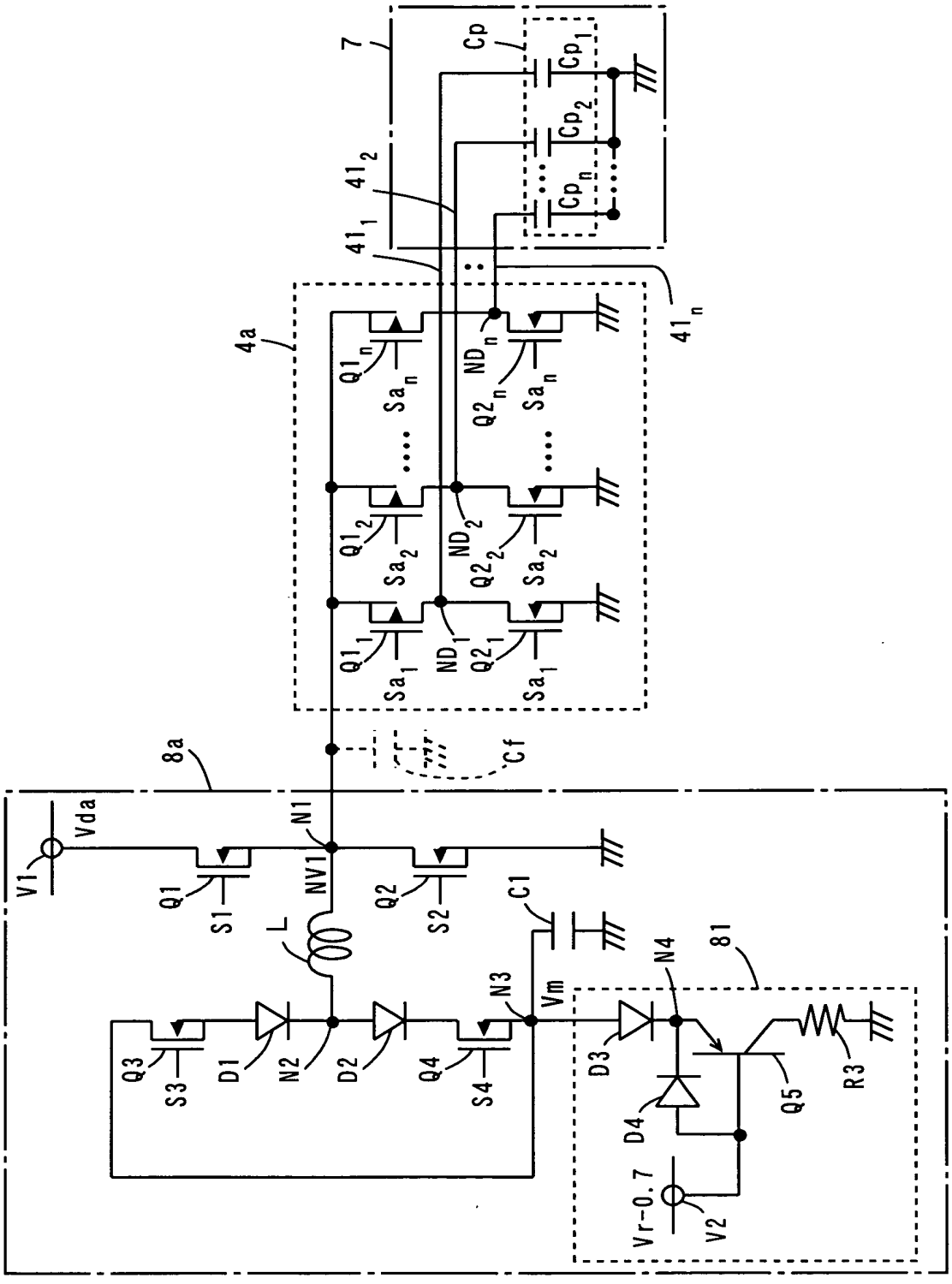

7
Cp
Cp1
Cp2
Cpn
41n
41n
41n
4a
Q1n
San
NDn
Q2n
Q12
Sa2
ND2
Q22
Q11
Sa1
ND1
Q21
Cf
8a
Vda
V1
N1
NV1
Q1
S1
Q2
S2
C1
L
Q3
S3
D1
N2
D2
Q4
S4
N3
Vm
81
N4
D3
D4
Q5
R3
Vr-0.7
V2

FIG. 22

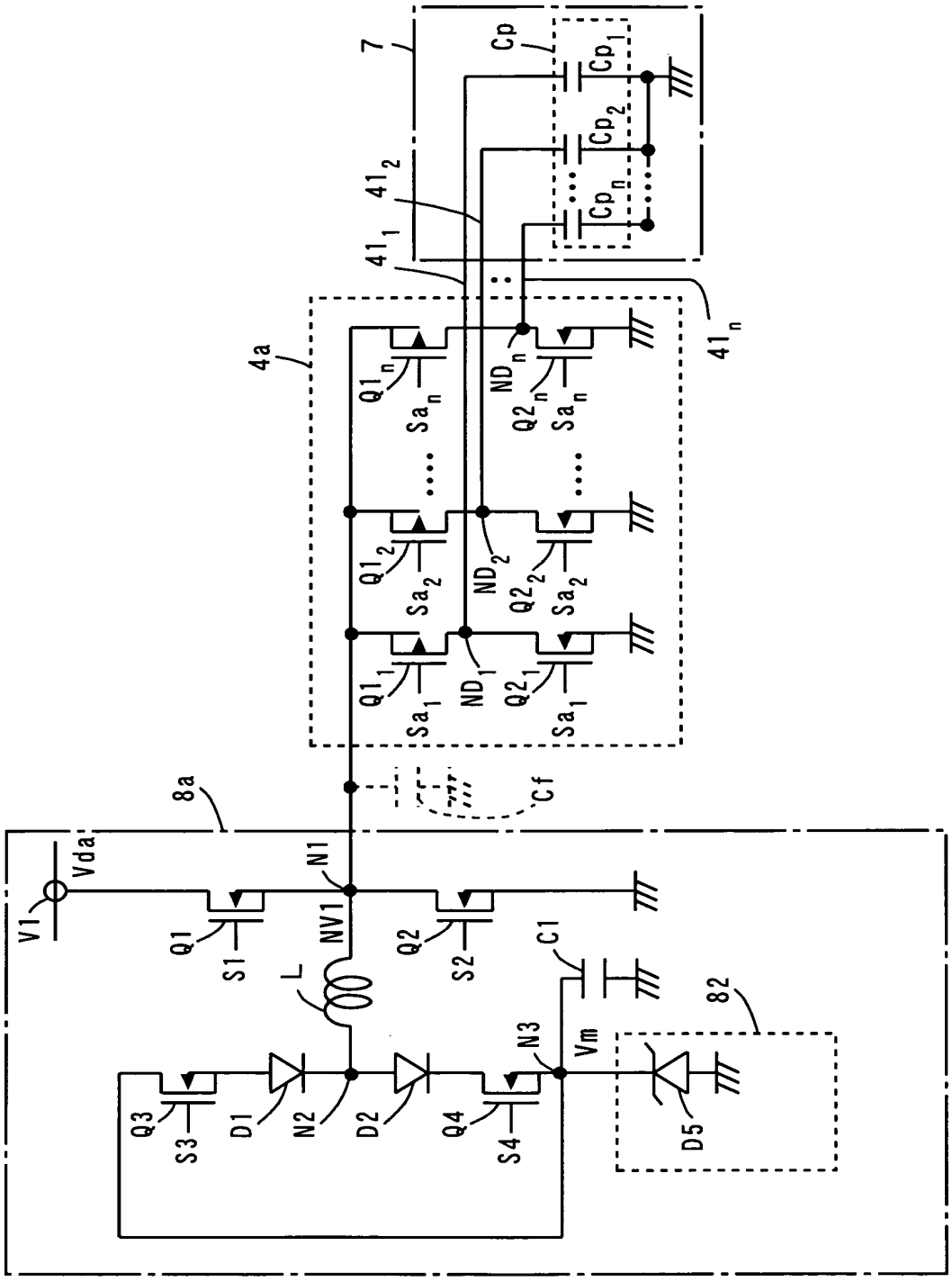
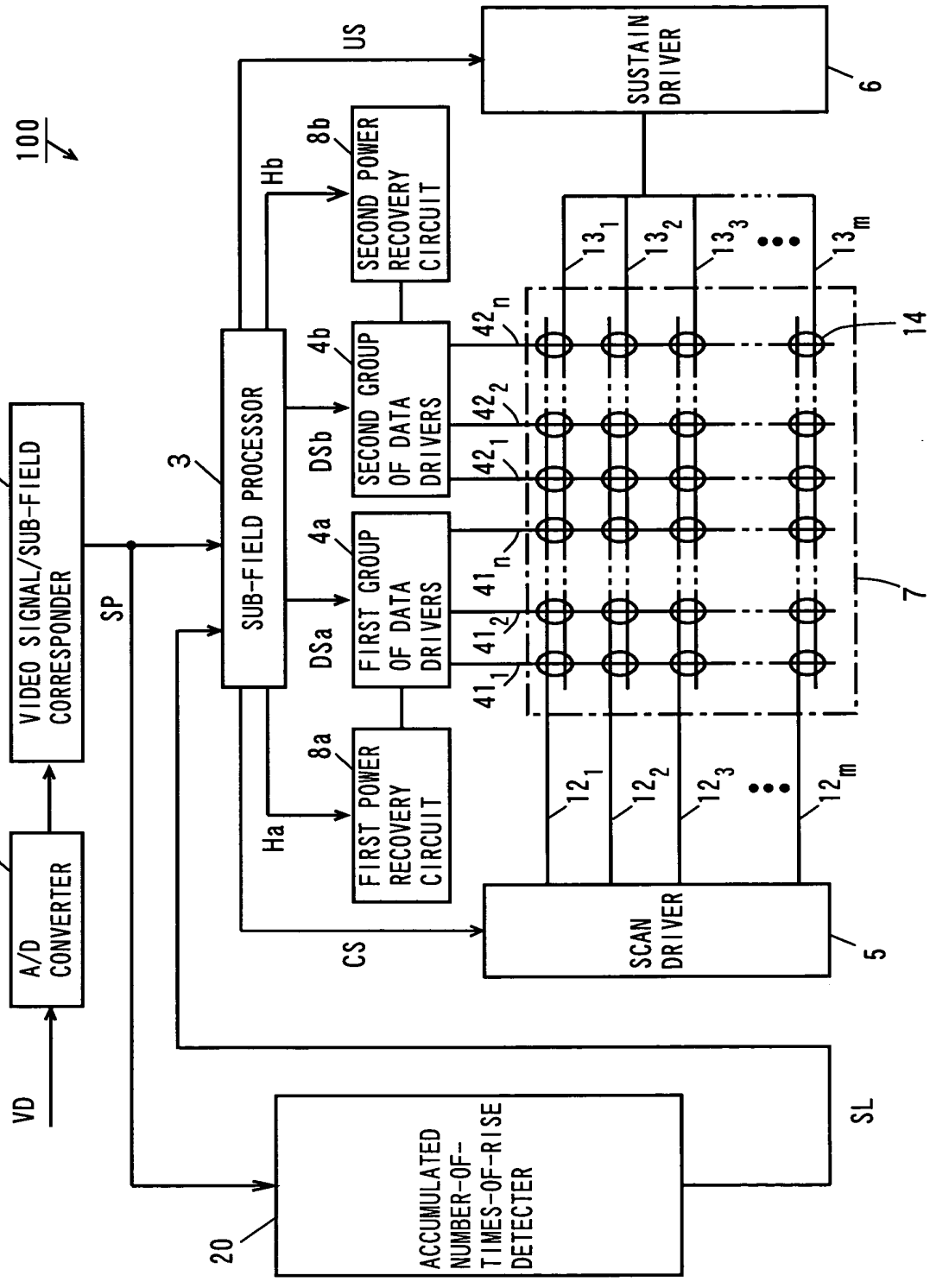

7
Cp
Cp1
Cp2
Cpn
41 2
41 1
41 n
4a
Q1n
Sa n
NDn
Q2n
Sa n
Q12
Sa2
ND2
Q22
Sa2
Q11
Sa1
ND1
Q21
Sa1
Cf
8a
Vda
V1
N1
Q1
S1
NV1
Q2
S2
L
C1
82
N3
Vm
Q3
S3
D1
N2
D2
Q4
S4
D5

FIG. 23


100
VD
A/D CONVERTER
1
VIDEO SIGNAL/SUB-FIELD CORRESPONDER
2
SP
SUB-FIELD PROCESSOR
3
Ha
Hb
US
CS
SL
FIRST POWER RECOVERY CIRCUIT
8a
SECOND POWER RECOVERY CIRCUIT
8b
FIRST GROUP OF DATA DRIVERS
4a
SECOND GROUP OF DATA DRIVERS
4b
DSa
DSb
SUSTAIN DRIVER
6
SCAN DRIVER
5
ACCUMULATED NUMBER-OF-TIMES-OF-RISE DETECTER
20
7
14
41_1
41_2
41_n
42_1
42_2
42_n
12_1
12_2
12_3
12_m
13_1
13_2
13_3
13_m

F I G. 2 4

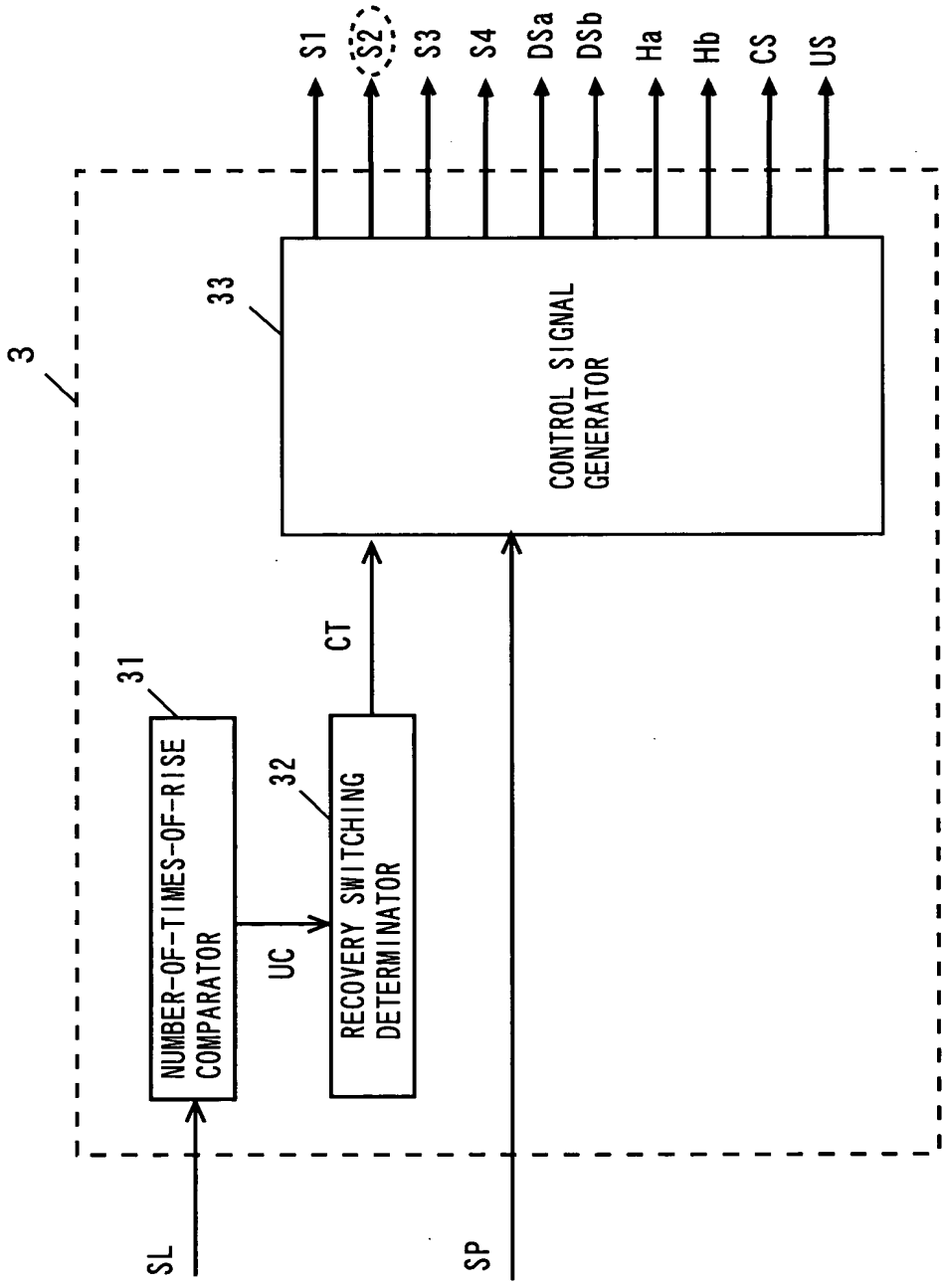

3
33
CONTROL SIGNAL GENERATOR
S1
S2
S3
S4
DSa
DSb
Ha
Hb
CS
US
31
NUMBER-OF-TIMES-OF-RISE COMPARATOR
32
RECOVERY SWITCHING DETERMINATOR
UC
CT
SL
SP

FIG. 25

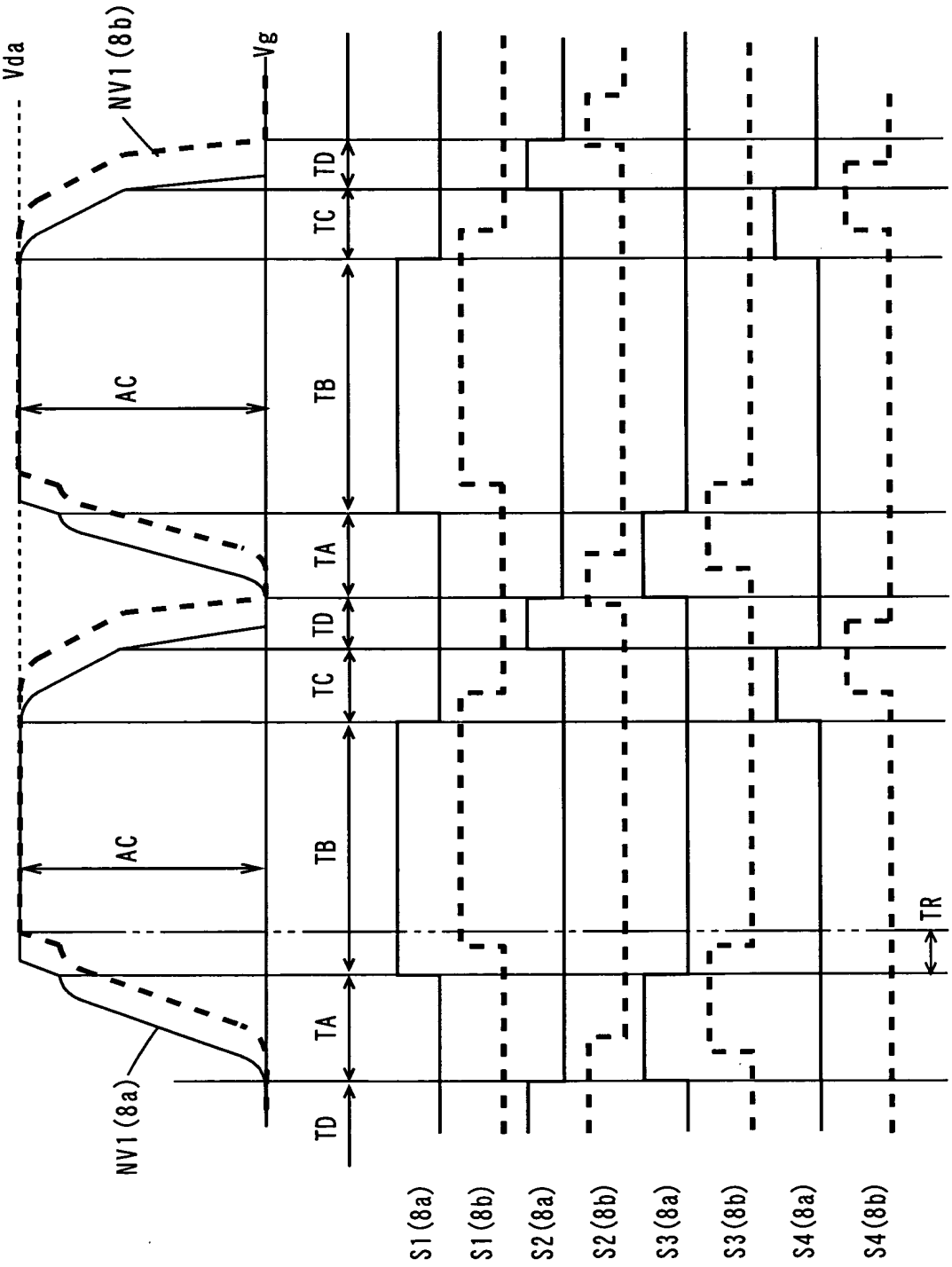

Vda
NV1(8b)
Vg
TD
TC
AC
TB
TA
TD
TC
AC
TB
TA
TD
NV1(8a)
TR
S1(8a)
S1(8b)
S2(8a)
S2(8b)
S3(8a)
S3(8b)
S4(8a)
S4(8b)

FIG. 26

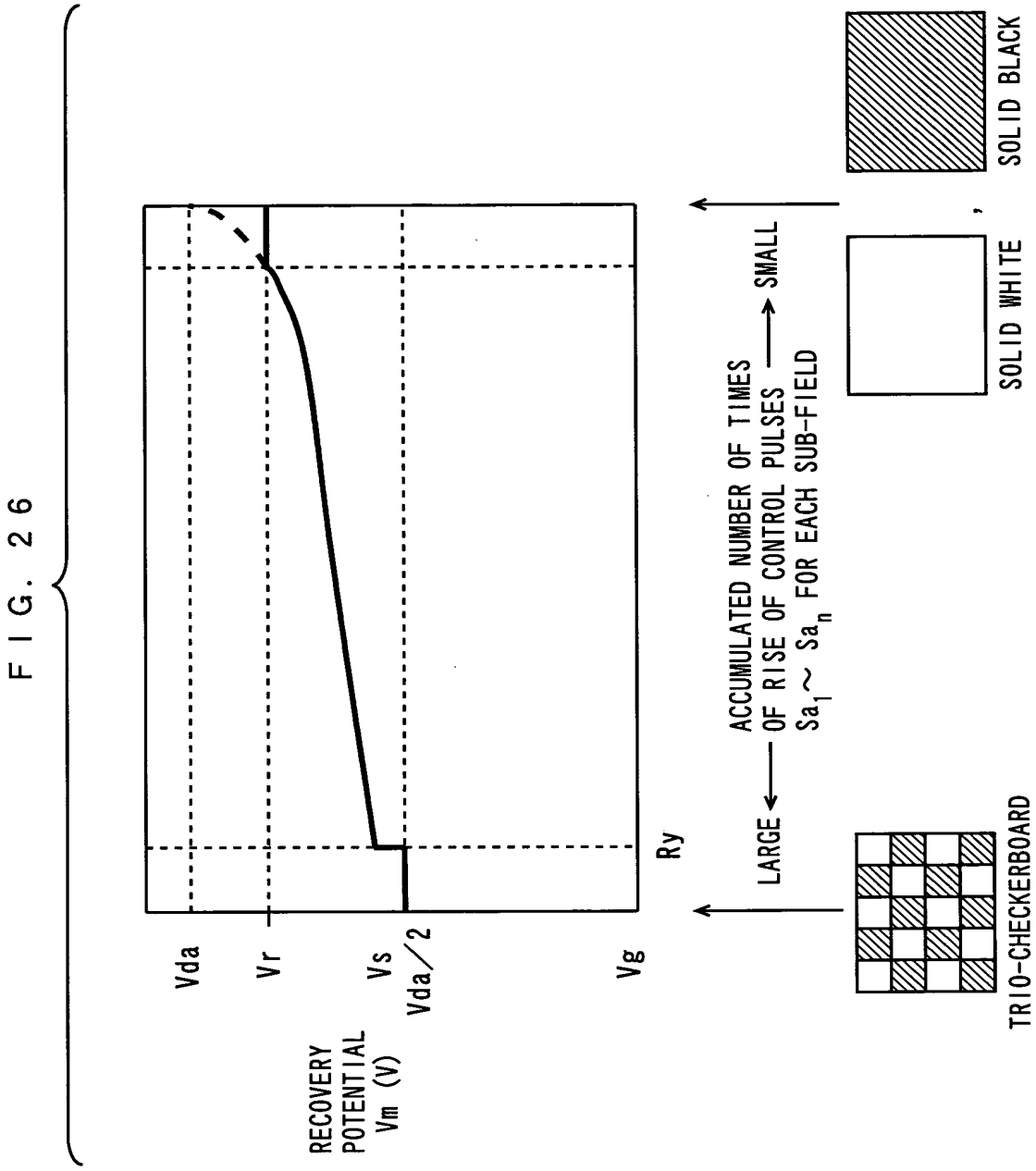

Vda
Vr
Vs
Vda/2
Vg
RECOVERY POTENTIAL Vm (V)
Ry
LARGE ← ACCUMULATED NUMBER OF TIMES OF RISE OF CONTROL PULSES → SMALL
$Sa_1 \sim Sa_n$ FOR EACH SUB-FIELD
TRIO-CHECKERBOARD
SOLID WHITE
SOLID BLACK

FIG. 27

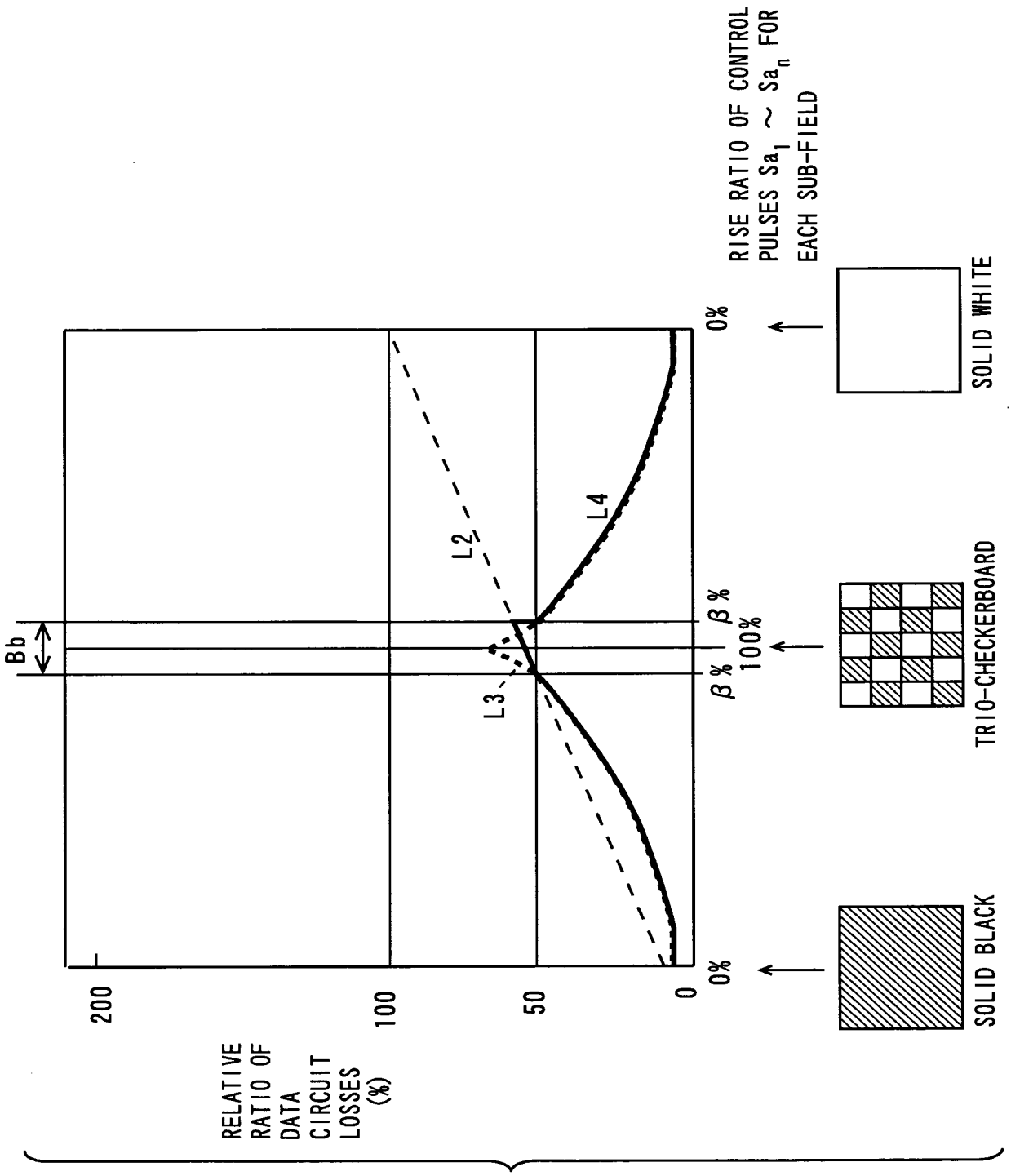

RELATIVE RATIO OF DATA CIRCUIT LOSSES (%)
200
100
50
0
Bb
L2
L3
L4
0%
β%
100%
β%
0%
RISE RATIO OF CONTROL PULSES $Sa_1 \sim Sa_n$ FOR EACH SUB-FIELD
SOLID BLACK
TRIO-CHECKERBOARD
SOLID WHITE

FIG. 28

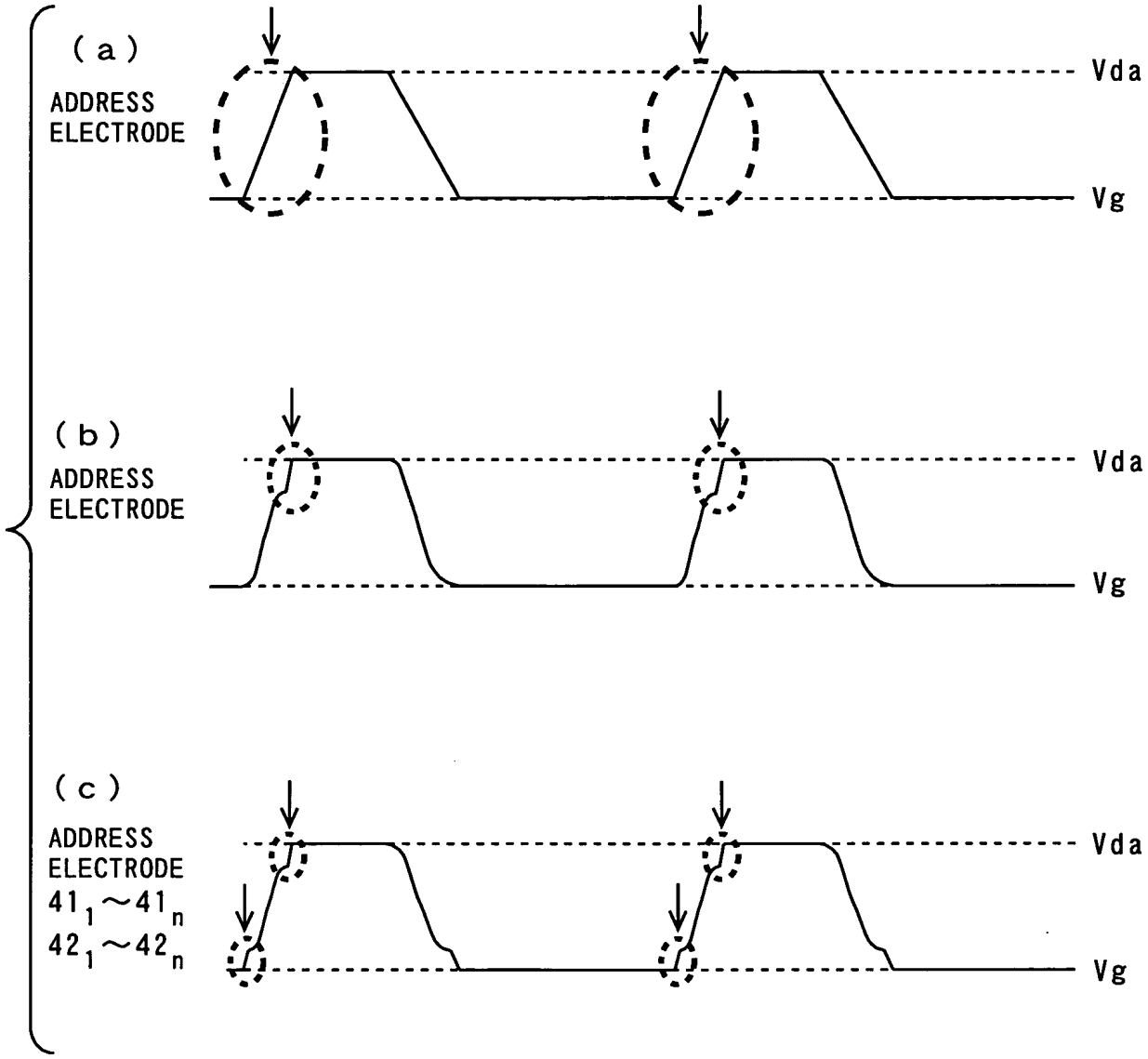

(a)
ADDRESS ELECTRODE
Vda
Vg
(b)
ADDRESS ELECTRODE
Vda
Vg
(c)
ADDRESS ELECTRODE
41$_1$～41$_n$
42$_1$～42$_n$
Vda
Vg

FIG. 29 PRIOR ART

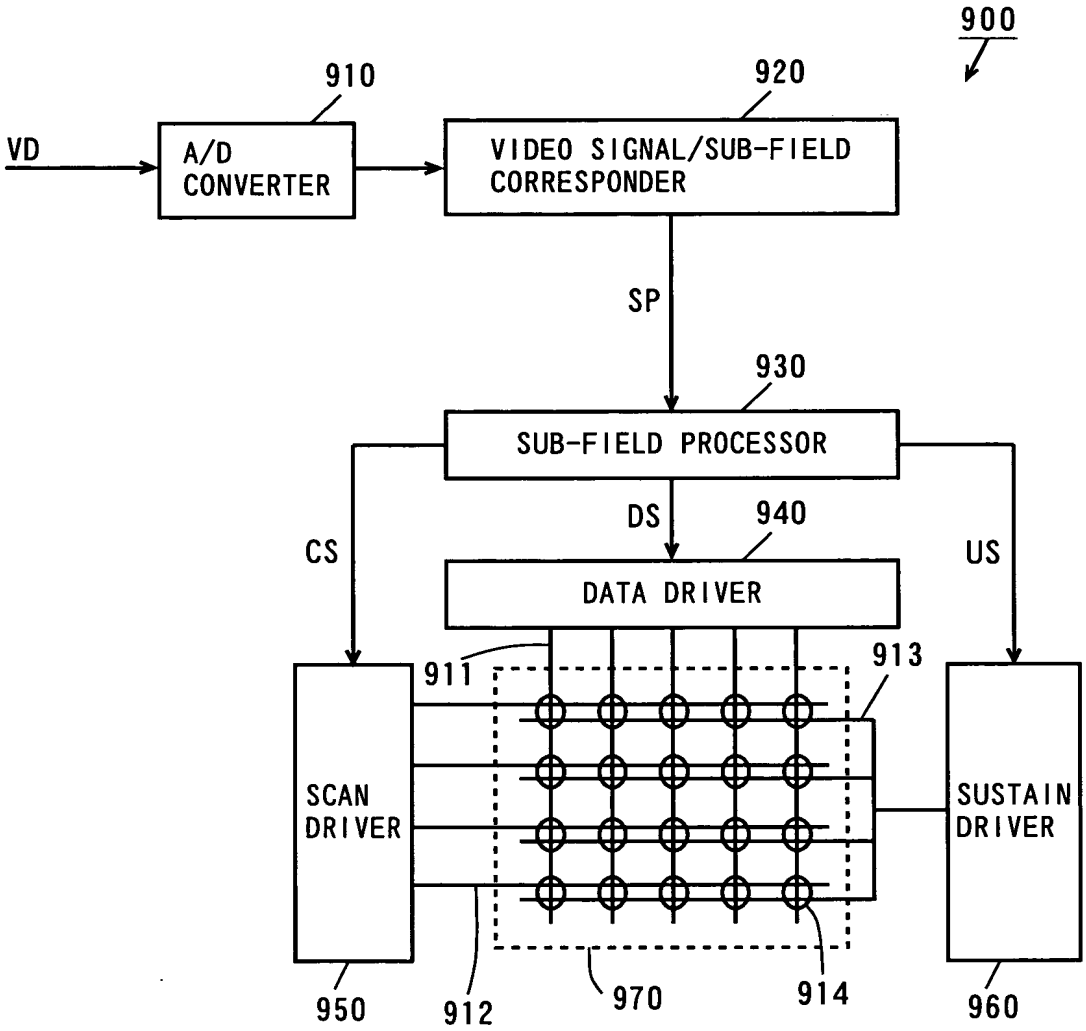


FIG. 30 PRIOR ART

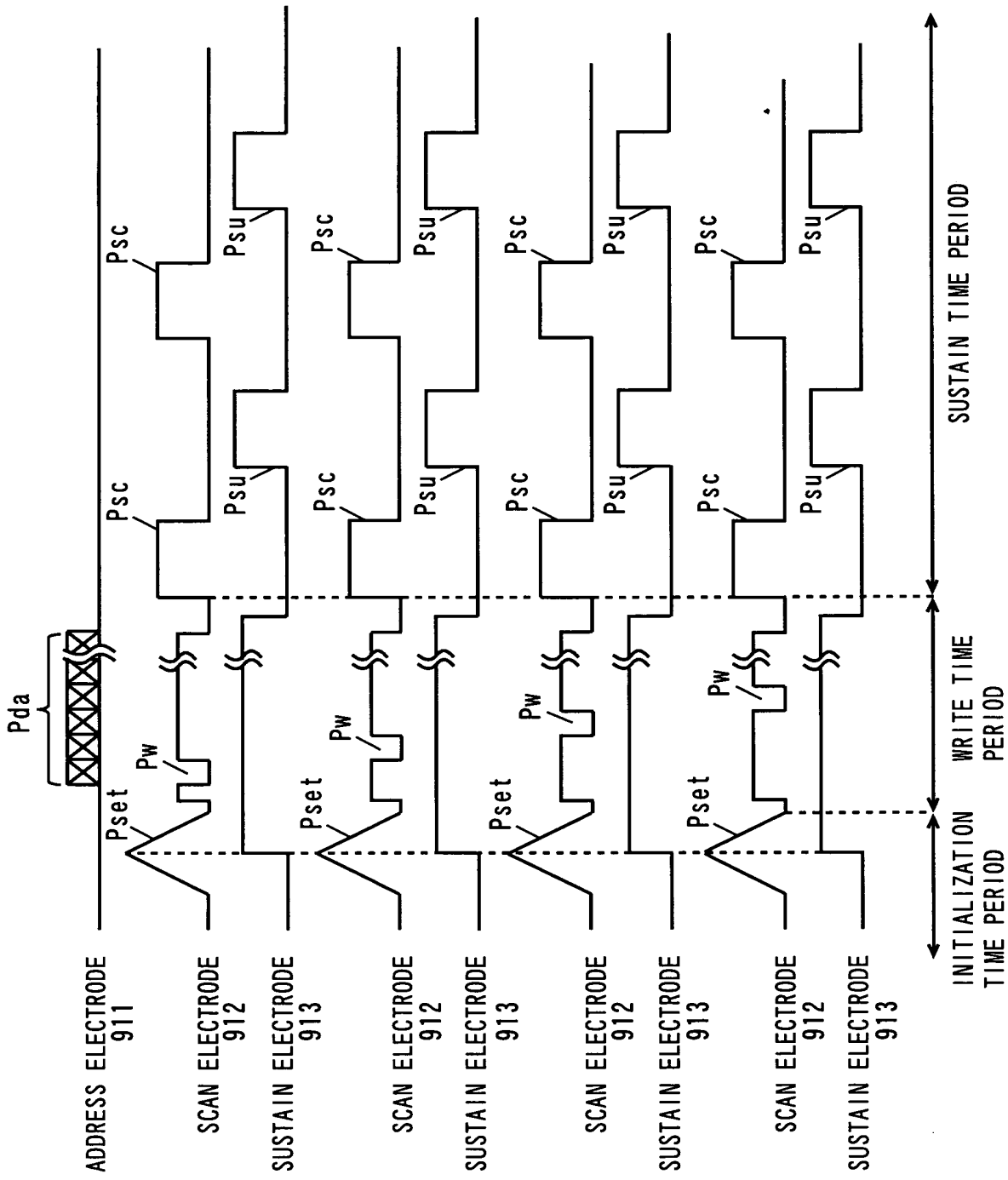


FIG. 31 PRIOR ART

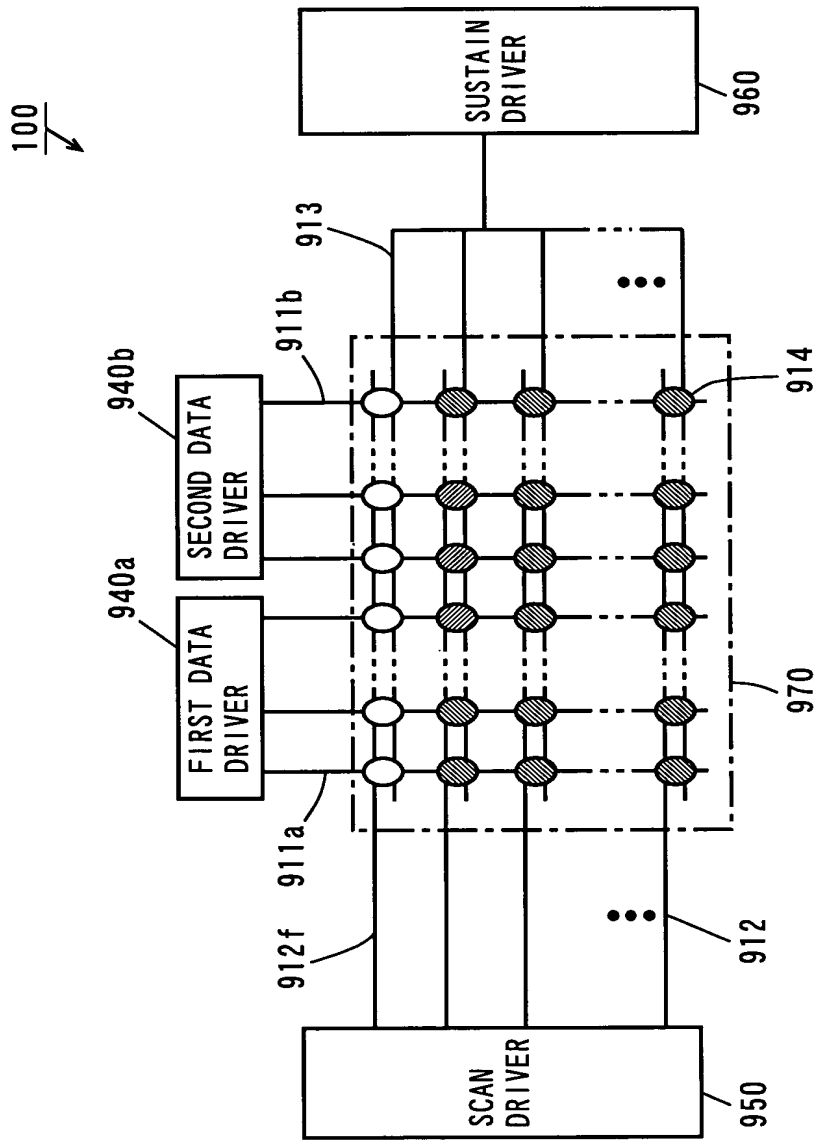


FIG. 32 PRIOR ART

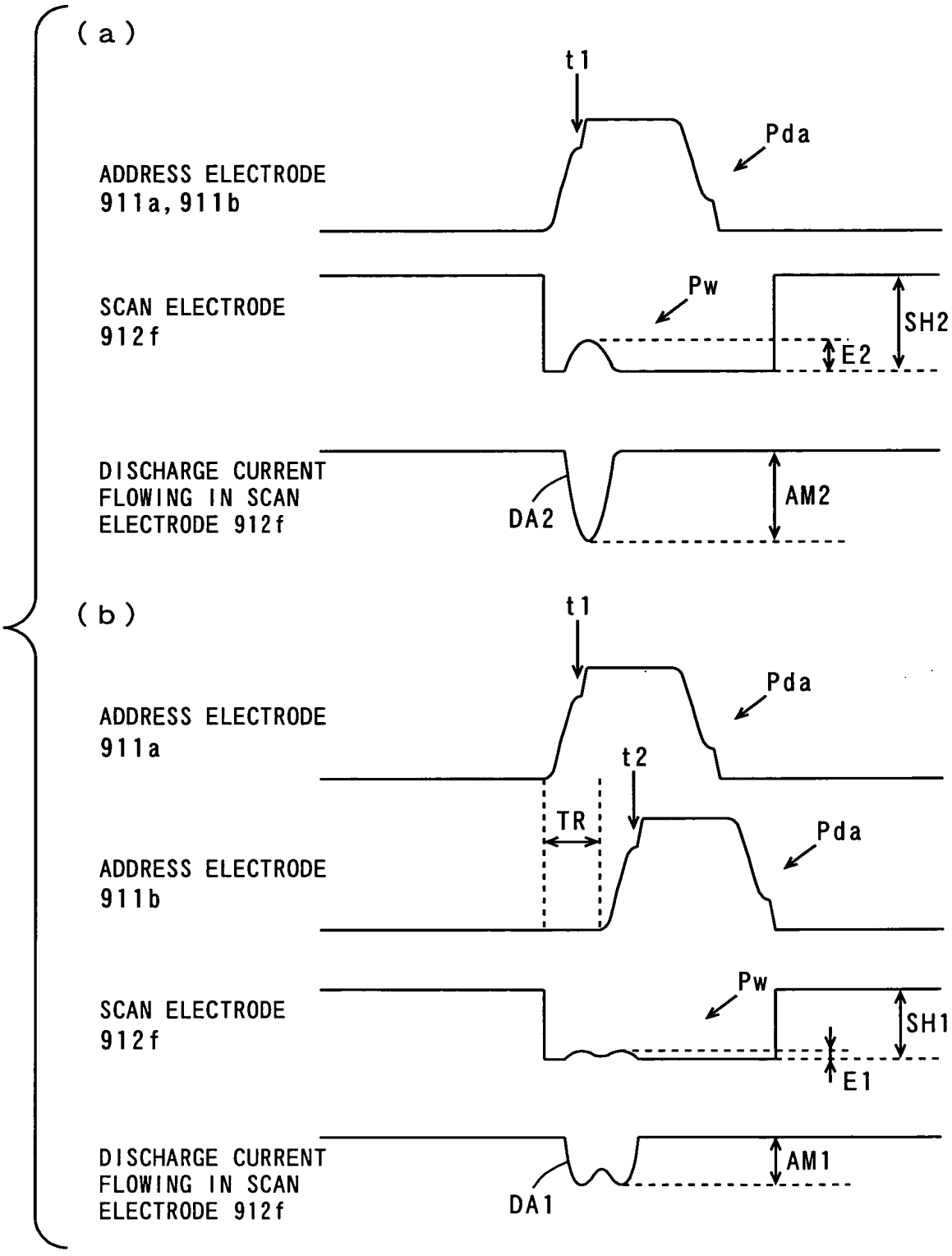


FIG. 33 PRIOR ART

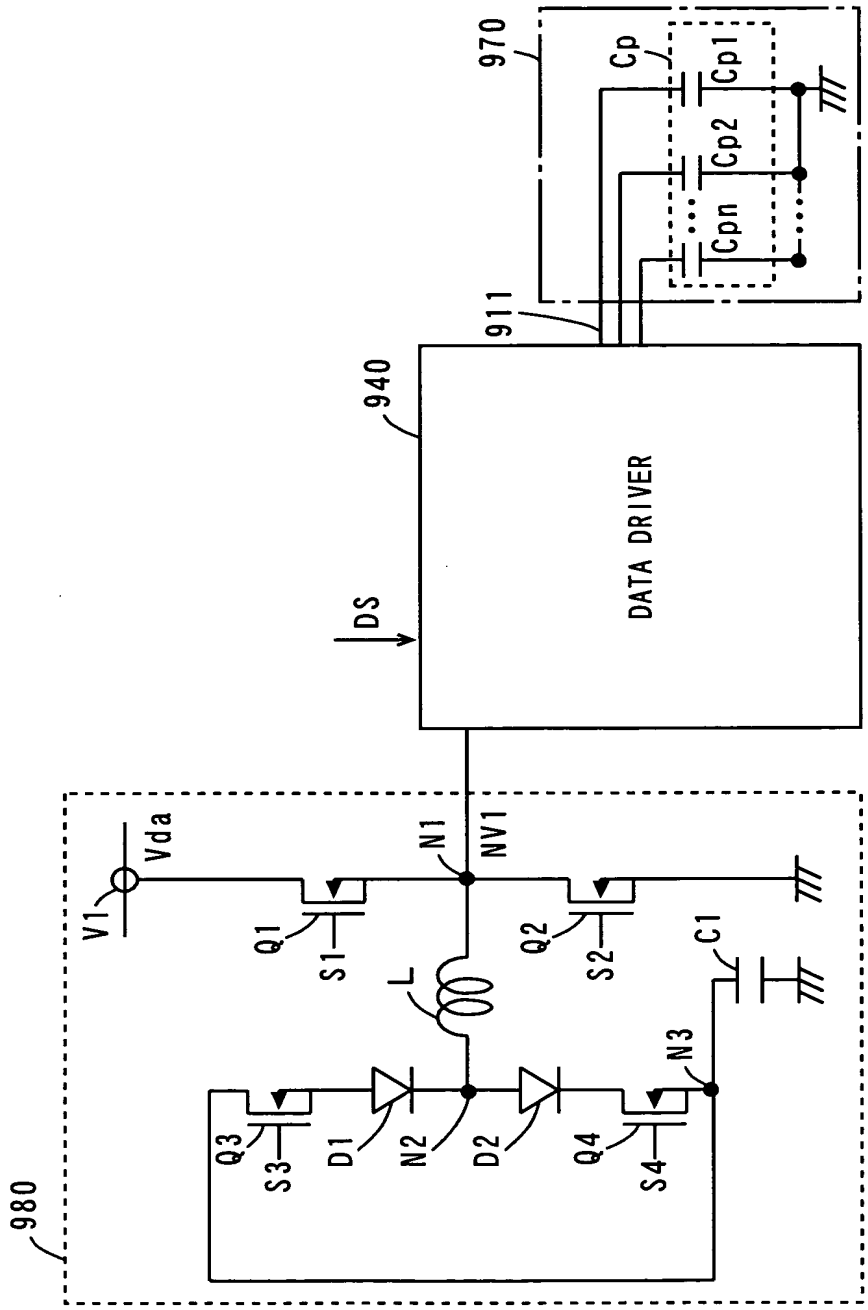


FIG. 34 PRIOR ART

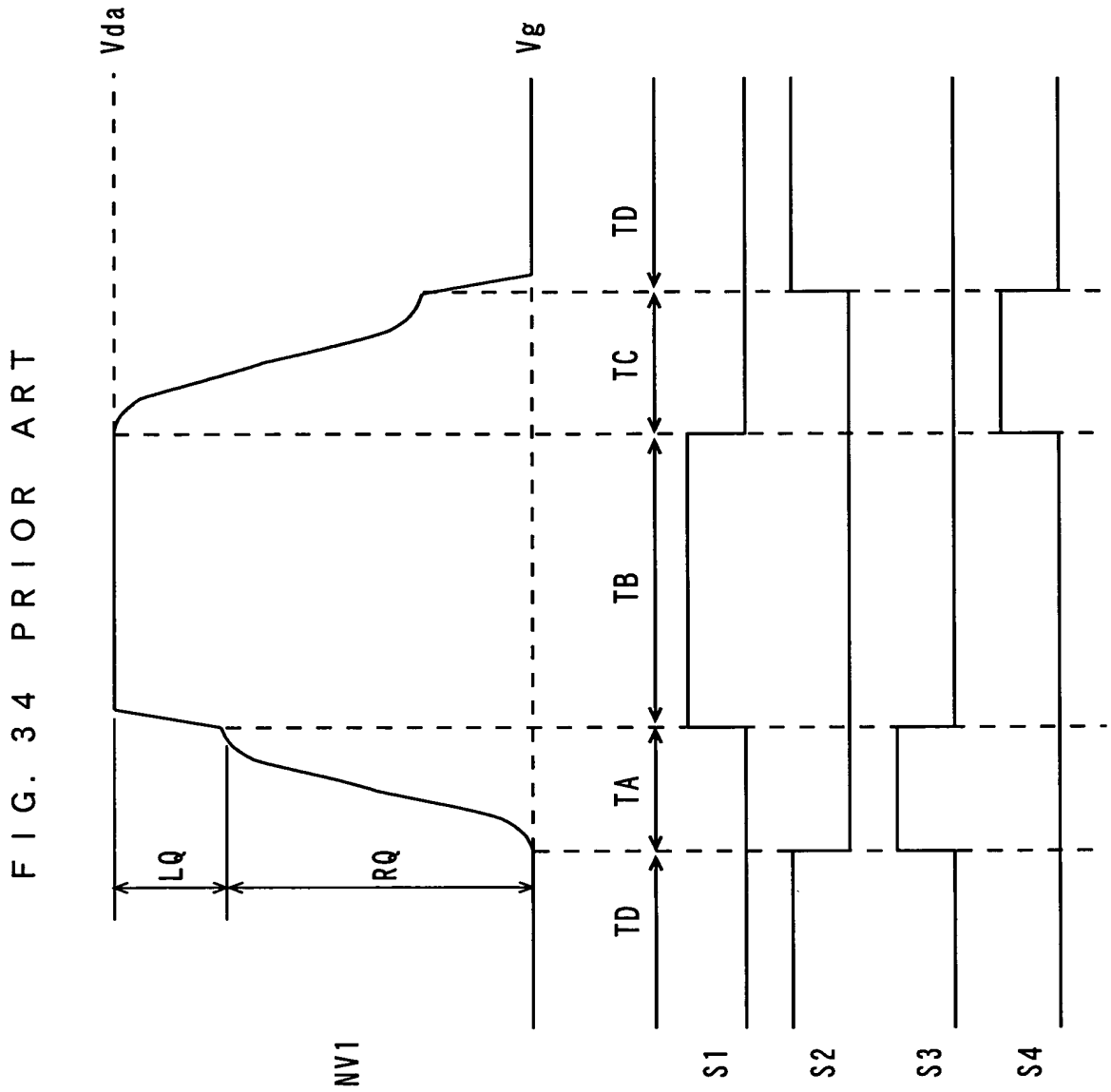


FIG. 35 PRIOR ART

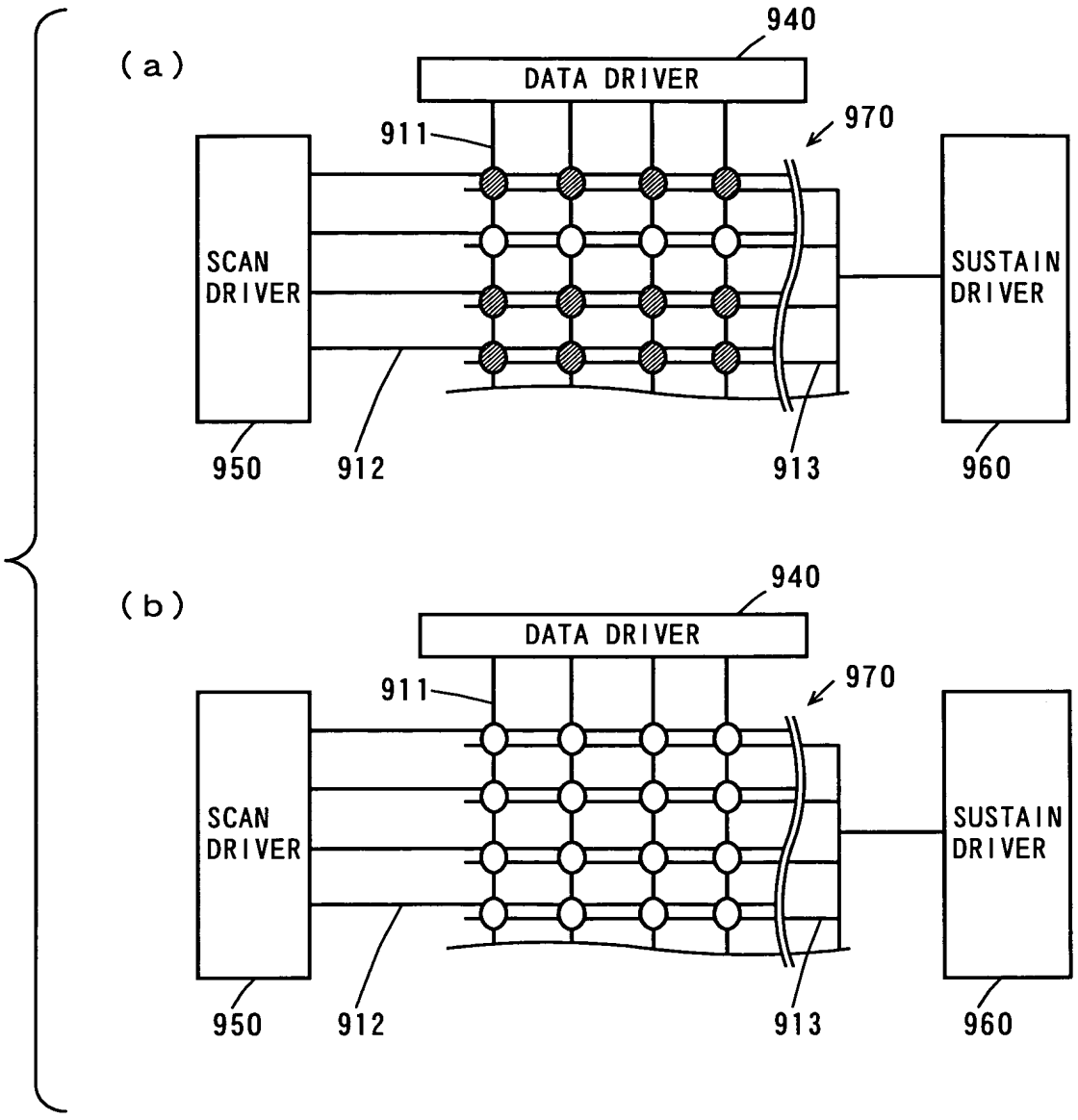
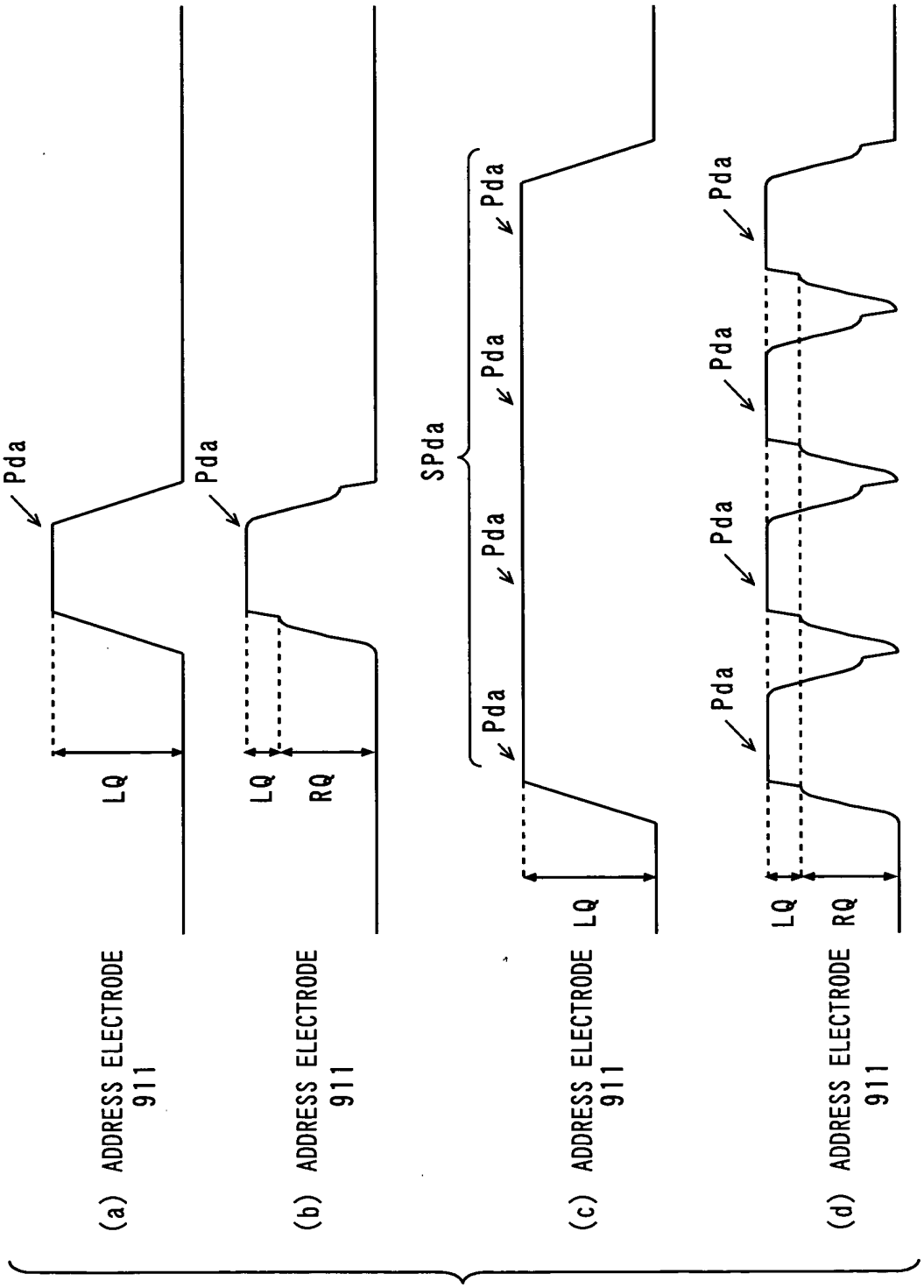



FIG. 36 PRIOR ART